POWER QUALITY IMPROVEMENT USING UPQC

[1]Prof. P. M. Akotkar, [2]Prof. P. G. Bhende
Assistant Professor, Department of Electrical Engineering, MSOET,Akola(M.S.), India[1] , Associate Professor, Department of Electrical Engineering, MSOET, Akola (M.S.), India[2]
akotkarpriya35@gmail.com,[1] pravinbhende10@gmail.com[2]

ABSTRACT

Power Quality (PQ) problem mostly refers to Voltage sag, ltage and source current problems and enhance power quality of the system. In this study the performance of new topology of UPQC namely open UPQC is investigated for the mitigation of balanced and unbalanced voltage sag, voltage swell and source current harmonics. The configurations of open UPQC namely Right Shunt Open UPQC (OUPQC-R) is analyzed with various control techniques .In this paper the capability of the OUPQC-R to enhance the power quality with reference generation and control techniques like Unit Vector Template (UVT) and Instantaneous p-q (PQ) is investigated. Various combinations of these techniques are also analyzed for the configuration of open UPQC. Simulation results carried out by using MATLAB simulink.

Keywords— unified power- quality conditioner (UPQC), pq problems, sensitive load, non linear load.

1. INTRODUCTION

The nature of electric power supply is mostly affected by the wide application of power electronic based equipment. Uninterrupted sinusoidal voltage at desired frequency and magnitude should always be provided to the consumers. On the other hand consumers should draw sinusoidal current. Many researchers are taking effort for the effective improvement of power quality. UPQC is considered as the most powerful custom power device to mitigate the problems arising due to power quality. It is necessary to take care of supply voltage disturbances such as voltage sag/swells, voltage flickers, load reactive power as well as voltage and current harmonics. UPQC is a combination of series and shunt active power filter (APF) connected through a common DC link capacitor. The series APF is connected to the supply line through a series transformer. The series APF prevents the source side voltage disturbances from entering into the load side to make the load voltage at desired magnitude and frequency on the other hand the shunt APF connected in parallel across the load limits the current related problems to the load side to make the current from the source purely sinusoidal. In this paper two different control schemes are used for series and shunt APF.

2. MODELING OF UPQC

The series APF prevents the source side voltage disturbances from entering into the load side to make the load

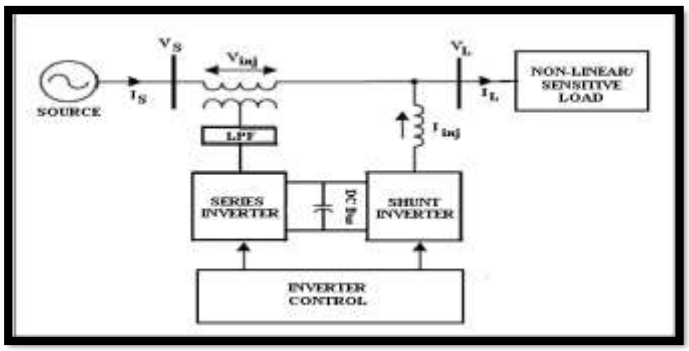


Figure.1. Configuration of UPQC

voltage at desired magnitude and frequency on the other hand the shunt APF connected in parallel across the load limits the current related problems to the load side to make the current from the source purely sinusoidal. In the recent year's utility as well as end users are seems to be more concerned about the quality of power. Increased use of sensitive loads and emphasis on energy efficiency resulting into excessive use of nonlinear loads are the major challenges in maintaining good power quality voltage swell and harmonics. UPQC can simultaneously mitigate load vo

2.1 SHUNT ACTIVE FILTER

The shunt active filter has a Voltage Source Inverter (VSI), Interfacing Inductor, and ripple filter. The design of VSI includes the DC bus voltage level, the DC capacitance and the rating of IGBTs used. The design of Interfacing Inductors and the Ripple Filter is presented here. The design is carried out considering a right shunt UPQC. The DC capacitor connected at the DC bus acts as energy buffer and provides dc voltage for the normal operation of the shunt APF. The DC bus voltage $V_{DC,}$ DC a bus capacitance $C_{DC,}$ interfacing inductors (Lf), and voltage and current rating of switches are calculated as below.

2.2 SELECTION OF THE DC BUS VOLTAGE

The minimum DC bus voltage of VSC of shunt APF should be greater than twice the peak of phase voltage of the distribution system. The DC bus voltage is calculated as

$$V_{DC=}2^{*}\ 2\sqrt{2}*V_{LL}/\sqrt{3}\ \text{m} \qquad 1$$

Where m is modulation index and considered 1 and V_{LL} is the AC line output voltage of the shunt APF, during transient the energy conservation is applied as

$$1/2*C_{DC}*\left(V_{DC}{}^{2}-V^{2}{}_{DC1}\right)=K_{1}3VaIt \qquad 2$$

Where V_{dc} is the nominal DC voltage equal to the reference DC voltage and V_{dc1} is the minimum voltage level of the DC bus , α is the overloading factor, V is phase voltage, I is the phase current, and t is the time by which the Dc bus voltage is to be recovered.

2.3 INTERFACING INDUCTOR

The AC inductance (L_f) of a VSI depends on the current ripple, $I_{cr,pp,}$ switching frequency f_s and DC voltage (V_{dc}), and it is given as

$$L_f = \sqrt{3}mV_{dc}/12\alpha f_s I_{cr,pp,} \qquad 3$$

Where m is the modulation index and α is the overloading factor.

2.4 DC LINK VOLTAGE

The minimum DC bus voltage of the VSI of the UPQC should be greaterthan twice of the peak of the phase voltage of the distribution system. The DC bus voltage as

$$V_{DC} = 2\sqrt{2}V_{LL}/\sqrt{3}m \qquad 4$$

Where m is the modulation index and is considered is 1 and V_{LL} is the Ac output voltage of the shunt APF. Thus V_{DC} is selected as 700 V as for V_{LL} is 415V.

2.5 RIPPLE FILTER

A small capacity rated RC filter is connected in parallel with the interfacing inductor to eliminate the high switching ripple content in the series active injected voltage ,the ripple filter is designed considering the cut off frequency of 5 kHz. The time constant of the filter should be very small compared with the fundamental time period (T), $R_fC_f<<T/1$, where R_f and C_f are the ripple filter resistance and its capacitance, respectively. Considering a low impedance of 8.1 Ω for the harmonic voltage at frequency of 5 kHz, the ripple filter capacitor is designed as C_f = 5μf. A series resistance (R_f) of 0.5Ω is included in series with the capacitor (C_f).

2.6 DESIGN OF SERIES ACTIVE FILTER (DVR)

The basic function of the series active filter is to inject voltage V_{DVR} generated by converter in series to the bus voltage by using an injection transformer. The temporary magnitudes of the three injected phase voltages are controlled such as to eliminate any disadvantageous effects of a bus fault to the load voltage . This means transient disturbances causes Differential voltage in the ac feeder will be compensated by an equivalent voltage generated by the converter and injected on the medium voltage level through the injection transformer.

2.7 SELECTION OF INJECTION TRANSFORMER

The function of the injection transformer is to increase the voltage supplied by the filtered VSI output to the desired level. The transformer winding ratio is pre-determined according to the voltage essential in the secondary side of the transformer. The injection transformer is selected for connecting the VSI of a series active filter in series with the supply. For compensation a voltage variation 30 %, the voltage to be injected is calculated as.

$$V_{DVR} = XSs \quad (5)$$

The DC bus voltage 700 V can be used to obtain 415 V across the line at the output of the VSI using a PWM controller. However, the UPQC required 65.81 V per phase. Therefore, the maximum value of the turns of the injection transformer is

$$K_{DVR} = V_{VSC} / V_{DVR} \quad (6)$$

The VA rating of the injection transformer is

$$S_{DV} = 3\, V_{DVR}\, I_{DVR\ (under\ sag)} \quad (7)$$

2.8 SELECTION OF DC LINK CAPACITOR

The value of Dc capacitor (C_{dc}) of the VSC of the series active filter depends on the instantaneous energy available to the series active filter during unbalance condition. The principal of energy conservation is applied as

$$½ * C_{dc}(V^2dc - V^2dc1) = k_1 3V\alpha It \quad (8)$$

Where V_{dc} is the nominal DC voltage and V_{dc1} is the minimum voltage level of the DC bus α is the overloading factor, V is phase voltage, I is the phase current.

2.9 DC LINK VOLTAGE

The minimum DC bus voltage of the VSI of the UPQC should be greater than twice of the peak of the phase voltage of the distribution system. The DC bus voltage is given as

$$V_{DC} = 2\sqrt{2}V_{LL}/\sqrt{3}m \quad (9)$$

Where m is the modulation index and is considered is 1 and V_{LL} is the Ac output voltage of the UPQC.

Thus V_{DC} is selected as 700 V as for V_{LL} is 415V.

3. PRAPOSED METHOEDOLOGY

3.1 UNIT VECTOR TEMPLATE (UVT) TECHNIQUE FOR SERIES CONTROL

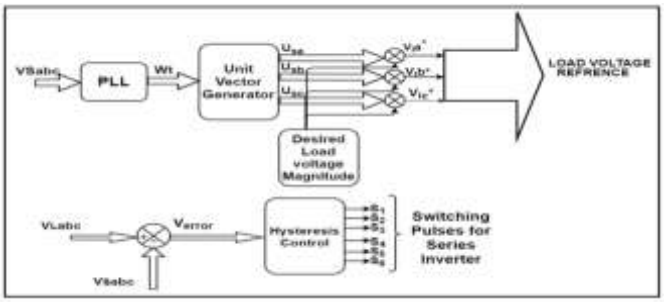


Figure.2. UVT Control Technique for generation of reference Voltage

Three phase unbalanced supply voltages are sensed and given to the PLL which generates two quadrature unit vectors (sinθ, cosθ). The two quadrature in phase unit vector of PLL are used to compute the supply in phase, 120^0 displaced three unit vectors (ua, ub, uc) using equation.

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -1/2 & -\sqrt{3}/2 \\ -1/2 & \sqrt{3}/2 \end{bmatrix} \begin{bmatrix} \sin\theta \\ \cos\theta \end{bmatrix} \quad 10$$

The extracted unit vector templates are then multiplied with the desired peak value of the PCC phase voltage (V^*lm) and generates the three-phase reference PCC voltages as:

$$\begin{bmatrix} u_a^* \\ u_b^* \\ u_c^* \end{bmatrix} = V_{LM}^* \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \quad 11$$

The desired peak value of phase voltage at PCC is calculated from equation (12) as,

$$V_M = \sqrt{\frac{2}{3}(V^2_{sa} + V^2_{sb} + V^2_{sc})} \quad 12$$

The computed voltages are then given to the comparator along with the sensed three-phase PCC voltages. The error generated is then taken to hysteresis controller to generate the required switching signals to the series APF. The series APF thus maintains the PCC voltage constant.

3.2 UNIT VECTOR TEMPLATE (UVT) TECHNIQUE FOR SHUNT CONTROL.

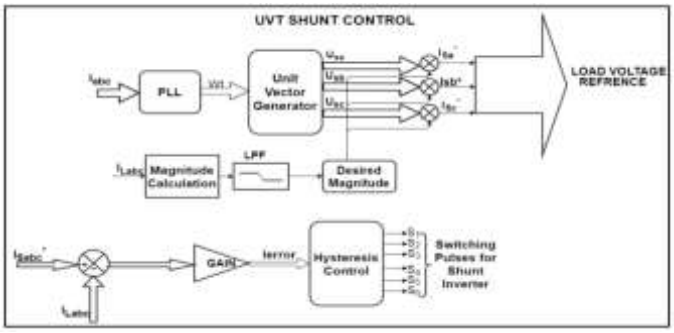


Figure.3.UVT Control Technique for generation of reference Current

The amplitude of the reference supply current (I^*SP) is computed by using equation (12) in terms of current .The three phase reference supply currents are computed by multiplying their magnitude (I∗sp) and in- phase unit current vectors as

$$\begin{pmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{pmatrix} = I^*_{SP} \begin{pmatrix} u_a \\ u_b \\ u_c \end{pmatrix} \quad 13$$

the sensed supply currents compared with reference supply current and the computed error signals are given to a hysteresis current controller to generate the switching signals to the switches of the shunt active filter which makes the supply currents follow its reference values.

3.3 INSTANTANEOUS P-Q TECHNIQUE FOR UPQC FOR SHUNT CONTROL

Instantaneous p-q technique is used for the control of shunt inverter of UPQC in order achieve mitigation of source current harmonics.

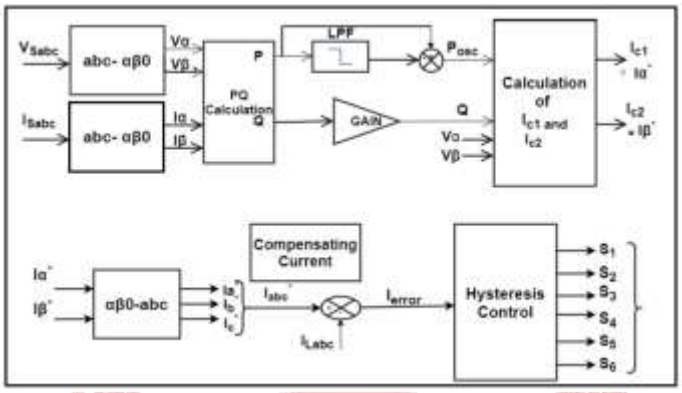


Figure.4. Generation of Reference current by p-q method

The control requires to measure source current I_{Sabc} and source voltage V_{Sabc} from the system in order estimate a reference current using instantaneous p-q technique. Source voltage and current are transformed to αβ0 reference using (12) and (13)

$$\begin{bmatrix} V_0 \\ V_\alpha \\ V_\beta \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} \sqrt{1/3} & \sqrt{1/3} & \sqrt{1/3} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3/2} & -\sqrt{3/2} \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \quad 12$$

$$\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3/2} & -\sqrt{3/2} \end{bmatrix} \begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} \quad 13$$

In the recent year's utility as well as end users are seems to be more concerned about the quality of power. Increased use of sensitive loads and emphasis on energy efficiency resulting into excessive use of nonlinear loads are the major challenges in maintaining good power quality voltage swell and harmonics. UPQC can simultaneously mitigate load vo

3.4 SHUNT ACTIVE FILTER

The shunt active filter has a Voltage Source Inverter (VSI), Interfacing Inductor, and ripple filter. The design of VSI includes the DC bus voltage level, the DC capacitance and the rating of IGBTs used. The design of Interfacing Inductors and the Ripple Filter is presented here. The design is carried out considering a right shunt UPQC. The DC capacitor connected at the DC bus acts as energy buffer and provides dc voltage for the normal operation of the shunt APF. The DC bus voltage $V_{DC,}$ DC a bus capacitance $C_{DC,}$ interfacing inductors (Lf), and voltage and current rating of switches are calculated as below.

3.5 SELECTION OF THE DC BUS VOLTAGE

The minimum DC bus voltage of VSC of shunt APF should be greater than twice the peak of phase voltage of the distribution system. The DC bus voltage is calculated as

$$V_{DC=} 2* 2\sqrt{2} * V_{LL} / \sqrt{3}\ m \quad (1)$$

Where m is modulation index and considered 1 and V_{LL} is the AC line output voltage of the shunt APF, during transient the energy conservation is applied as

$$1/2 * C_{DC} * \left(V_{DC}{}^{2} - V^{2}{}_{DC1}\right) = K_1 3VaIt \quad (2)$$

Where V_{dc} is the nominal DC voltage equal to the reference DC voltage and V_{dc1} is the minimum voltage level of the DC bus , α is the overloading factor, V is phase voltage, I is the phase current, and t is the time by which the Dc bus voltage is to be recovered.

3.6 INTERFACING INDUCTOR

The AC inductance (L_f) of a VSI depends on the current ripple, $I_{cr,pp,}$ switching frequency f_s and DC voltage (V_{dc}), and it is given as

$$L_f = \sqrt{3} m V_{dc} / 12 \alpha f_s I_{cr,pp,} \quad (3)$$

Where m is the modulation index and α is the overloading factor.

3.7 DC LINK VOLTAGE

The minimum DC bus voltage of the VSI of the UPQC should be greaterthan twice of the peak of the phase voltage of the distribution system. The DC bus voltage as

$$V_{DC} = 2\sqrt{2} V_{LL} / \sqrt{3} m \quad (4)$$

Where m is the modulation index and is considered is 1 and V_{LL} is the Ac output voltage of the shunt APF. Thus V_{DC} is selected as 700 V as for V_{LL} is 415V.

3.8 RIPPLE FILTER

A small capacity rated RC filter is connected in parallel with the interfacing inductor to eliminate the high switching ripple content in the series active injected voltage ,the ripple filter is designed considering the cut off frequency of 5 kHz. The time constant of the filter should be very small compared with the fundamental time period (T), $R_fC_f << T/1$, where R_f and C_f are the ripple filter resistance and its capacitance, respectively. Considering a low impedance of 8.1 Ω for the harmonic voltage at frequency of 5 kHz, the ripple filter capacitor is designed as C_f = 5μf. A series resistance (R_f) of 0.5Ω is included in series with the capacitor (C_f).

3.9 DESIGN OF SERIES ACTIVE FILTER (DVR)

The basic function of the series active filter is to inject voltage V_{DVR} generated by converter in series to the bus voltage by using an injection transformer. The temporary magnitudes of the three injected phase voltages are controlled such as to eliminate any disadvantageous effects of a bus fault to the load voltage . This means transient disturbances causes Differential voltage in the ac feeder will be compensated by an equivalent voltage generated by the converter and injected on the medium voltage level through the injection transformer.

3.10 SELECTION OF INJECTION TRANSFORMER

The function of the injection transformer is to increase the voltage supplied by the filtered VSI output to the desired level. The transformer winding ratio is pre-determined according to the voltage essential in the secondary side of the transformer. The injection transformer is selected for connecting the VSI of a series active filter in series with the supply. For compensation a voltage variation 30 %, the voltage to be injected is calculated as.

$$V_{DVR} = XSs \quad (5)$$

The DC bus voltage 700 V can be used to obtain 415 V across the line at the output of the VSI using a PWM controller. However, the UPQC required 65.81 V per phase. Therefore, the maximum value of the turns of the injection transformer is

$$K_{DVR} = V_{VSC} / V_{DVR} \quad (6)$$

The VA rating of the injection transformer is

$$S_{DV} = 3\, V_{DVR}\, I_{DVR\ (under\ sag)} \quad (7)$$

3.11 SELECTION OF DC LINK CAPACITOR

The value of Dc capacitor (C_{dc}) of the VSC of the series active filter depends on the instantaneous energy available to the series active filter during unbalance condition. The principal of energy conservation is applied as

$$½ * C_{dc}(V^2dc - V^2dc1) = k_1 3V\alpha It \quad (8)$$

Where V_{dc} is the nominal DC voltage and V_{dc1} is the minimum voltage level of the DC bus α is the overloading factor, V is phase voltage, I is the phase current.

3.12 DC LINK VOLTAGE

The minimum DC bus voltage of the VSI of the UPQC should be greater than twice of the peak of the phase voltage of the distribution system. The DC bus voltage is given as

$$V_{DC} = 2\sqrt{2}V_{LL}/\sqrt{3}m \quad (9)$$

Where m is the modulation index and is considered is 1 and V_{LL} is the Ac output voltage of the UPQC. Thus V_{DC} is selected as 700 V as for V_{LL} is 415V.

4. SIMULATION AND RESULTS

The simulation model for OUPQC-R configuration is discussed. Fig. shows a simulation model of right shunt open UPQC (OUPQC-R).It consists of a series inverter connected to the injection transformer. The secondary side of the injection transformer is connected in series with power system in between source and load and the primary side of injection transformer is connected to the inverter. A shunt inverter is connected in parallel with the load through interfacing inductor. Separate DC sources are provided to the series and shunt inverter. The filters are connected on both series and shunt inverter to eliminate the ripples of high frequency caused because

of inverter switching. This configuration is named as right shunt configuration because the shunt inverter is placed on the right side of the series inverter.

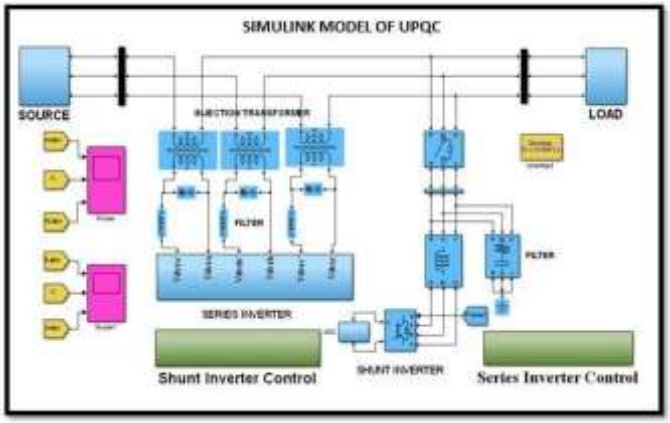


Figure.5. MATLAB Simulink model of OUPQC-R

Table.1.System and design parameters used for simulation

	Parameter	**Value**
Source	Voltage	415 Volts
	Frequncy	50 Hz
Load	Bridge Rectifier as nonlinear load	600 W
DC-link	Voltage (VDC)	700 V
	Capacitor (CDC)	600 µF
Series APF	Filter resistor and capacitor	8.1Ω , 5µF
Shunt APF	Filter resistor and capacitor	8.1Ω ,5 µF
	Interfacing Inductor	5.6 mH
Transformer	3 single phase transformer	1 kVA
Switching Frequency	Carrier Siganl (PWM)	1kHz

CASE 1: MITIGATION OF BALANCED AND UNBALANCED VOLTAGE SAG USING UVT TECHNIQUE

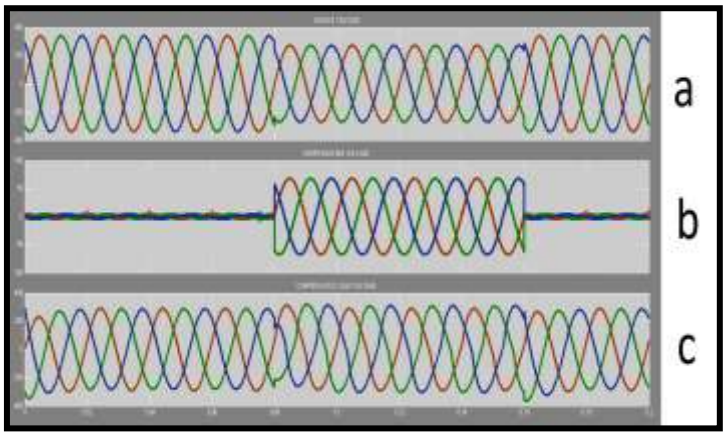


Figure.6. Results of mitigation of 20% balanced Voltage Sag
(a)Source Voltage (b) Compensating Voltage (c) Load Voltage

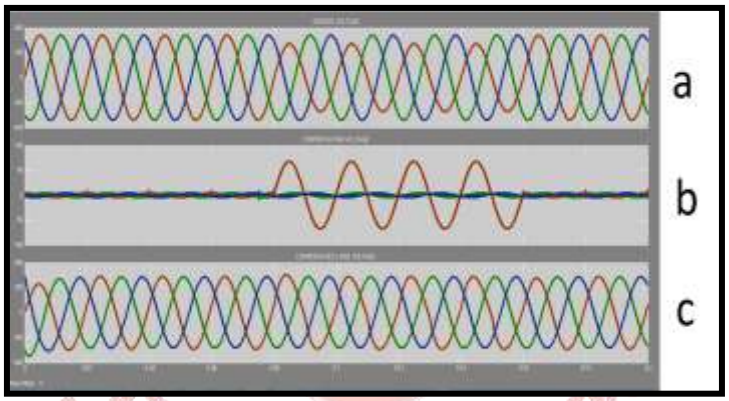


Figure.7. Results of mitigation of 20% unbalanced voltage sag
(a)Source Voltage (b) Compensating Voltage (c) Load Voltage

Case 1 refers to compensation of balanced and unbalanced voltage sag. Under this condition percentage of voltage sag is varied from 10% to 30%. The balanced voltage sag is obtained by varying the source voltage and reducing its magnitude for duration of four cycles. Fig. 6 shows the simulation result of mitigation of 20% balanced voltage sag. In this case balanced voltage sag of 20% is observed for the duration from 0.08 second to 0.16 second in Fig.6 (a). Fig.6.(b) shows the error estimated by the reference generation technique, Fig.6.4 (c) shows the compensated load voltage. The result shows that OUPQC-R can effectively compensate the balanced voltage sag.

For unbalance voltage sag that may be caused because of single line to ground fault. In this case unbalanced sag of 20% is obtained by varying source voltage of phase A. The magnitude of phase A is reduced by 20%. Fig.7 shows simulation result for compensation of 20% unbalanced voltage sag. From Fig.7 (a) it is observed that the voltage sag appears in phase A of the supply voltage for duration of four cycles from 0.08 second to 0.16 second. Fig.7 (b) shows an error or compensating voltage to be injected by series inverter of OUPQC-R in phase A. Fig.7 (c) shows load voltage after compensation.

CASE 2: MITIGATION OF VOLTAGE SWELL AND CURRENT HARMONICS USING UVT TECHNIQUE.

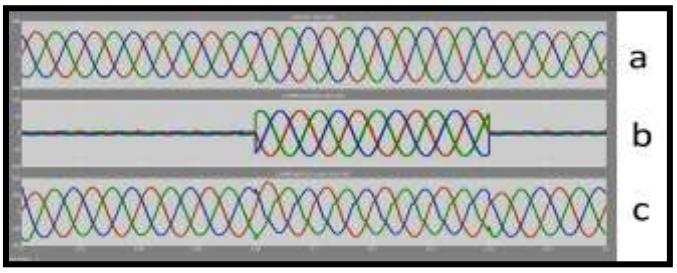


Figure.8. Results of compensation of voltage swell

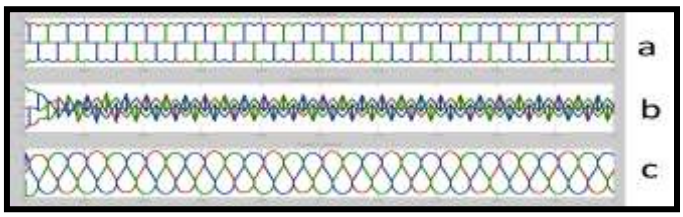


Figure.9. Results of compensation of current Harmonics

Case 2 refers to the analysis of right shunt open UPQC for voltage swell compensation and current harmonics mitigation. The figure.8 shows the simulation results of 20% voltage swell. the voltage swell is obtained by increasing the magnitude of all three phases for specific time. The fig. 8. (a) Shows the system voltage swell for the duration of four cycles from 0.08 to 0.16 second. Figure. 8 (b) shows the compensating voltage signal and Figure. 8 (c) shows the compensated load voltage. It can be observed from the result that UPQC can satisfactorily compensate the required magnitude of swell in voltage but a small distortion in load voltage is observed. The THD of load voltage is investigated and found to be 5.19% which is below the THD limit of 8% as stated by IEEE 519-2014.

Fig.9 shows simulation result of system current harmonics compensation. In this case shunt inverter of the OUPQC-R is turned ON from the beginning and the required compensating current is injected by device. Fig.9 (a) shows distorted load current of the rectifier system. Fig.9 (b) shows the error or compensating current to be injected in the system by OUPQC-R and Fig.9 (c) shows the compensated source current.

CASE 3. SIMULATION OF RIGHT SHUNT OPEN UPQC USING INSTANTANEOUS P-Q (PQ) TECHNIQUE

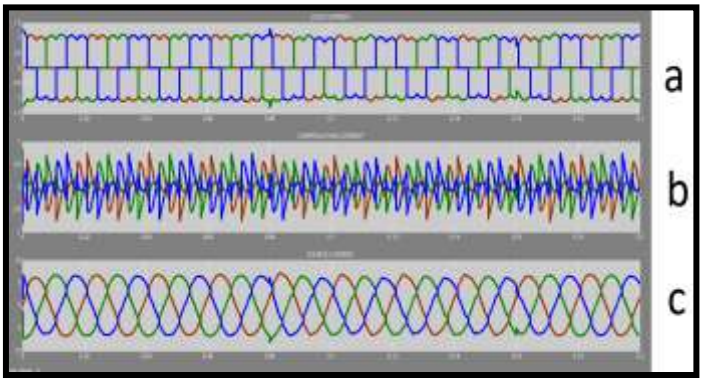
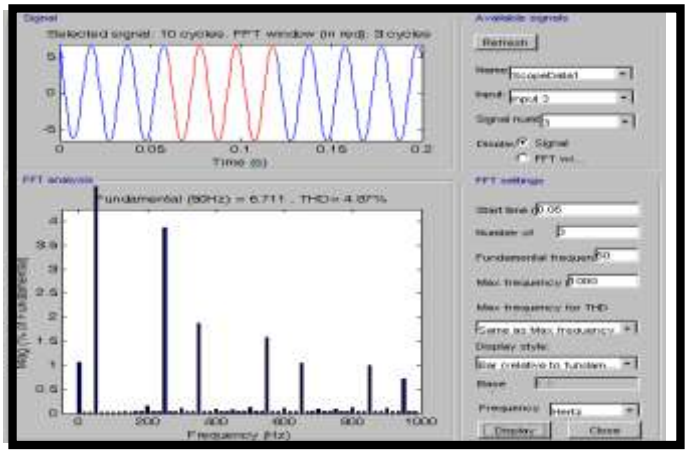


Figure.11. Simulation results of current Harmonics

(a) Load Current (b) Compensating Current (c) Source Current

Fig.11 shows simulation result of right shunt open UPQC using instantaneous p-q technique. The distorted load current is shown in Fig.11 (a).The compensating current required to be injected in the system is shown Fig.11 (b) and Fig.11 (c) shows compensated source current. The UPQC is turned ON from the beginning i.e. zero instant and it injects compensating current into system. The compensating current is in phase opposition to the



harmonic current present in the source current. This results in harmonic mitigation of source current.

Figure.12 THD Analysis of compensated load current

FFT analysis of the source current is carried and THD of the source current is determined to be 4.87%. it is evident from the result presented in Fig 11 and Fig. 12 that right shunt open UPQC with instantaneous p-q technique for reference current generation can effectively compensates the source current harmonics. The performance of the OUPQC-R for enhancement of current quality is found adequate.

TABLE.2. PERFORMANCE ANALYSIS OF RIGHT SHUNT OPEN UPQC

Factor for Performance Analysis	**Performance of Right Shunt Open UPQC**	
	UVT	**PQ**
Compensation of balanced Voltage Sag	10-30%	--
Compensation unbalanced Voltage Sag	10-30%	--
Compensation of Voltage Swell	10-30%	--
Compensation of Current Harmonics	**8.70%**	**4.87%**

5. CONCLUSION AND FUTURE SCOPE

It is observed from table that the OUPQC-R with the different control techniques (UVT and PQ) satisfactorily compensates the balanced voltage sag, in the range of 10% to 30%. It is also observed that the OUPQC-R with UVT technique can satisfactorily compensate unbalanced voltage sag in the range of 10% to 30%. It can be viewed from the table that OUPQC-R can effectively compensate voltage swell in the range of 10% to 30% with UVT technique used for series control. Whereas reduction of THD from 30% to 4.87% is obtain, when PQ

technique is used for shunt controller.It is also observed that reduction of THD from 8.75 % in UVT technique to 4.87% when PQ technique is used. The effectiveness of OUPQC-R configuration with UVT-PQ technique is required to be investigated experimentally. So in future an experimental study of OUPQC-R can be carried out.

REFERENCES

[1] Rosli Omar and NasrudinAbd Rahim "Mitigation of voltage sag/swell by using DVR" ARPN Journal of Engineering and Applied Sciences, vol. no 4, June 2009.

[2] Bhim Singh and venkateswarlu.P "A simplified control algorithm for three- phase , four wire unified power quality conditioner" Presented at journal of power electronics ,vol no.1, January 2010.

[3] S. N. Gohil, M.V.Makwana, K.T. Kadivar,G.J.Tetar "Three phase unified power quality conditioner(UPQC) for power quality improvement using UVTG Technique" 2013 International conference on renewable energy and sustainable energy [ICRESE'13].

[4] B.Singh, a chandra and k al haddad "review of active filters for power quality improvement" IEEE trans. Industrialelectronics,vol 46, No 5,pp.960-97, oct. 1999.

[5] Vijay Karale and SaurabhJadhao, "Voltage Sag Mitigation Using Dynamic Voltage Restorer" proceeding of 2nd International Conference on Innovations in Electrical and Electronics Engineering (ICIEEE); pp 184- 187, Aug 2015.

[6] V. S. Karale, S. S. Jadhao, M. Tasare, Dr. G. M. Dhole "UVTG Based Dynamic Voltage Restorer for Mitigation of Voltage Sag" , (Submitted for acceptance) In proceeding of International Conference 2015, Computing Communication Control and Automation (ICCUBEA), Pune.

[7]IEEE Std. 1159 – 1995, "Recommended Practice for Monitoring Electric Power Quality".

[8] P.Boonchiam and N. Mithulananthan, Thammasat "Understanding of Dynamic Voltage Restorers through MATLAB Simulation," Int. J. Sc. Tech., Vol. 11, No. 3, July-Sept 2006.

[9] R.C.Dugan, M.F.McGranaghan and H.W. Beaty, "Electrical Power Systems Quality". New York: McGraw-Hill, 1996.

[10] IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems, IEEE Standard 519-1992, 1992.(Standards and Reports)

E-ISSN NO:2349-0721