MEMORY TESTING MECHANISM: AN EAGLE EYE

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ABSTRACT

In order to fulfill the market need almost everyday novel products are through of and are developed using top-notched technology. The first and the foremost expectation from such products is, they are expected to be super quick. To make any product super responsive, the processing capacity and the storage component play equal and vital role. Apart from this, self-diagnosis has gaining significant place in the development of the smart products. The product capable of self-testing, reduces time to market, increases the live time and also prevent the possible data loss in case if failure occurs. Different testing mechanisms are employed to implement self-diagnosing procedures in the products. In this review paper we are about to disclose a detailed analysis on different methodologies reported for implementation of the self-diagnosis procedures.

Keyword: - Memory Testing, MBIST, BIST

1. INTRODUCTION

Memory testing mechanism is the additional circuitry developed to check the performance of the memory component in the system itself. This is additional circuit which is developed along with the system to check the performance of the memory component periodically. In this process, the known set of in put combinations are generated, which are called as the stimulus, and are applied to the memory under testing. With the known set of the input combinations, possible output combinations are also predictable. Hence, the recorded output after application of the input stimulus is compared with the expected output combinations and result is concluded. If the output combinations are same as the expected output combinations, then it is concluded that, the circuit is working properly, otherwise circuit is malfunctioning. The product with self-testing capability assures high reliability, so that, systems can be employed to control delicate applications such as aviation, autonomous car, weapon controlling, automatic guided vehicles, nuclear power plant and many other critical applications. Such modules are also incorporated to lower down the repair cycle. Such systems are way out where limited technician access is expected and to cut down the maintenance cost during manufacturing process.

2. MEMORY TESTING: REVIEW

The basic component in any FPGA device is the configurable logic blocks (CLBs). CLB is decoder like structure, which is used to store the logic to be configured in the FPGA after programming.

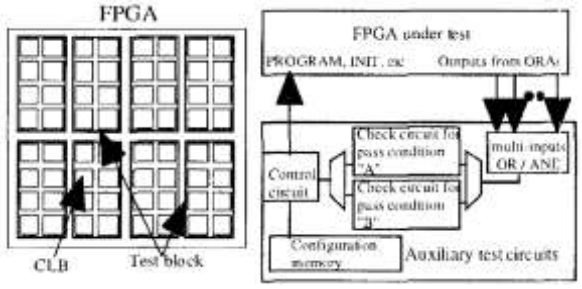


Fig -1 Test Blocks and Auxiliary Test Circuit

Authors in [1] have designed an architecture of Built in Self-Test for performance evaluation of configurable logic blocks. In the proposed architecture by the authors, since the FPGA is comprising of numerous CLBs which work parallelly, the test is performed simultaneously, for every test block of CLBs. Through this

proposed technique, authors have claimed that they have detected up to 5 faulty configurable logic blocks. The subsequent figure indicates the test blocks that us CLBs and Auxiliary Test Circuit mentioned by the authors.

On the other hand, authors in [2] have proposed built-in-self-test approach for digital clock manager available in Virtex 4 series FPGAs.

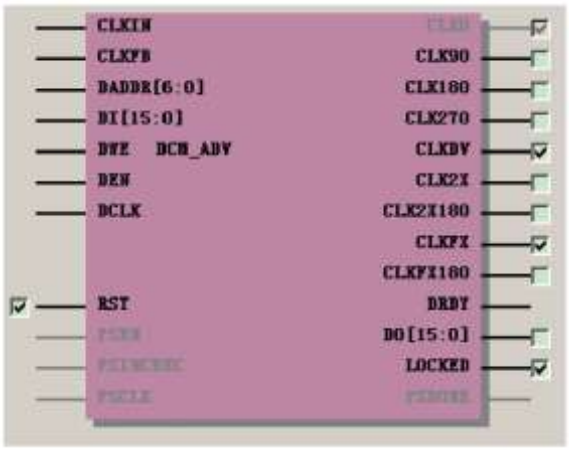
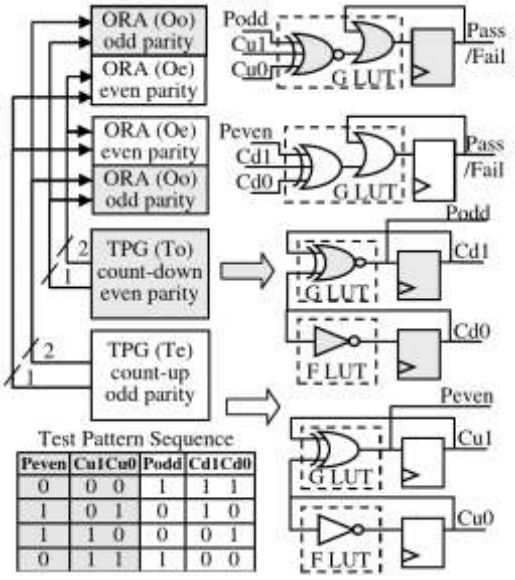


Fig -2. GUI of DCM in Virtex-4 FPGA

The proposed technique overcomes the drawbacks of the traditional ATE equipment of having tolerant to the minor errors and difficulty in passing high frequency components with integrity. So, the proposed technique detects even the minor errors using the alignment feature of the output clocks of Digital Clock Manager. In addition to this, frequency scanning mechanism which can check the frequency components.

Global routing resources are used for interconnecting CLBs and other significant components in the FPGA device for data and resource sharing. Authors [3] have disclosed cross coupled parity built in self test technique for the global routing resources in the programmable gate array device. Through this implemented system, authors have promised to verify the system level performance before configuration of the concurrent architecture, to come up with the reliable system. The subsequent figure discloses section of cross coupled parity routing built in self-test architecture.



Peven	Cu1Cu0	Podd	Cd1Cd0
0	0 0	1	1 1
1	0 1	0	1 0
1	1 0	0	0 1
0	1 1	1	0 0

Fig -3. Built in Self-Test Architecture for Routing Lines

In another approach, researchers [4] have disclosed a generic approach of built-in self-test implementation in FPGA. The target is to design a nonspecific skeleton of the BIST in FPGA architecture. This skeleton expected to be factory implemented in the FPGA architecture.

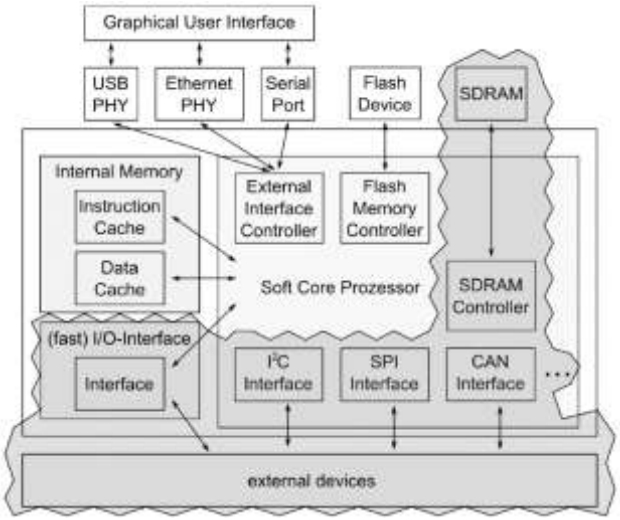


Fig -4. Proposed BIST Architecture of Embedded System and Its Peripherals

Later, using this pre-built generic BIST architecture whatever applications are designed, like digital television or other products, performance testing can be done by the user at their end using graphic user interface console provided by the system. The figure 4 discloses the BIST as a firmware.

One kind of BIST architecture is specifically designed to test the memory component. Authors have designed Memory Built in Self-Test component for testing the memory architecture in [5], as shown in figure 5. Authors have described the architecture using Very High-Speed Integrated Circuit Hardware Description Language (VHDL) and it is synthesized using Xilinx ISE platform. Verification of the proposed architecture is carried out by testing stuck at faults of SRAM.

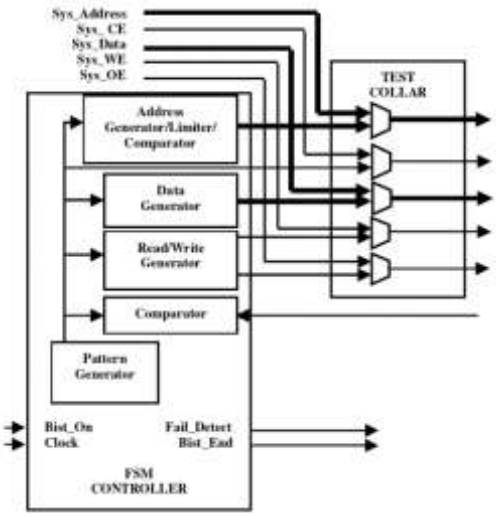


Fig -5. Proposed MBIST Controller

Performance evaluation of the Random-Access Memory (RAM) component is also possible, demonstrated by the authors in [6]. The said component of BIST is implemented using concurrent descriptive language like VHDL and is prototyped using Spartan-6 field programmable gate array. It is observed that, outcome of the simulation and outcome at the FPGA device have identical output. The architecture of the proposed design is as shown in figure 6 below.

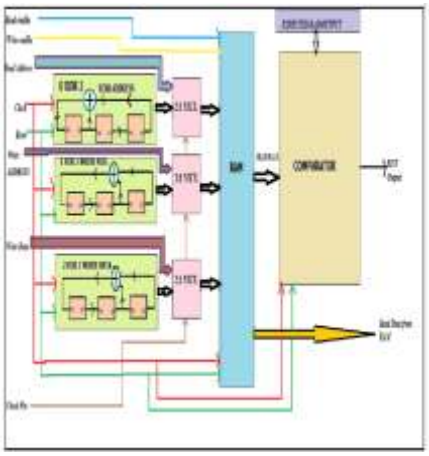


Fig -6. Internal View of The Proposed Design

Carry chains are used for performing few operations like addition, counting and others. To check the performance of the carry chain, researchers have implemented BIST scheme for FPGA in [7]. Here, the said architecture of the BIST is not computationally intensive, because the instead of generating the large number of random combinations, only required input possible combinations are generated and fed for system check. For implementation of the said design, the test of multiple bit adders is decomposed into test of single bit adders with carry considerations, as shown in figure 7.

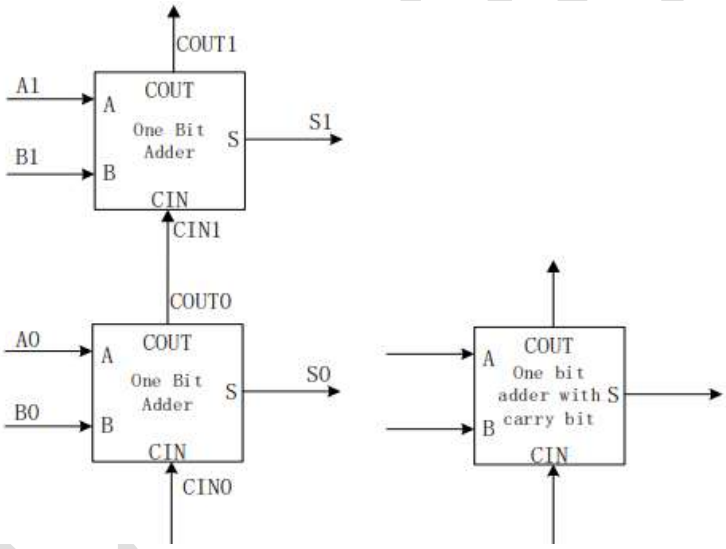


Fig -7. One- and Two-Bit Adder for The Said Design

Subsequently, authors [8] have tightly optimized and analysed the cheap polynomial fitting method for testing the analog to digital converter module. For optimization of the method, authors have used Code Simulink tool. The top-level architecture is then converted into a VHDL file, which is then can be used to prototype using FPGA or can be used to create built in component in ASIC approach.

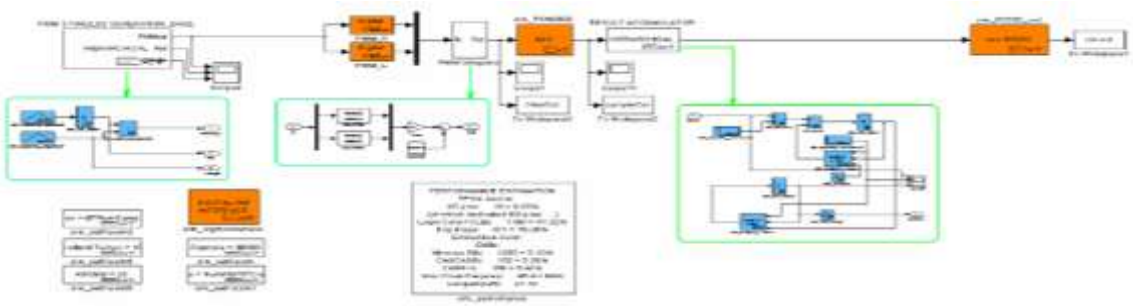


Fig -8. Code Simulink View of The Proposed Architecture

On the other hand, the Inter Integrated Circuit protocol with in-built self-testing capability is also proposed [9]. More simplified approach is used to implement the system through which no additional programming is needed for networking multiple devices through the I2C protocol.

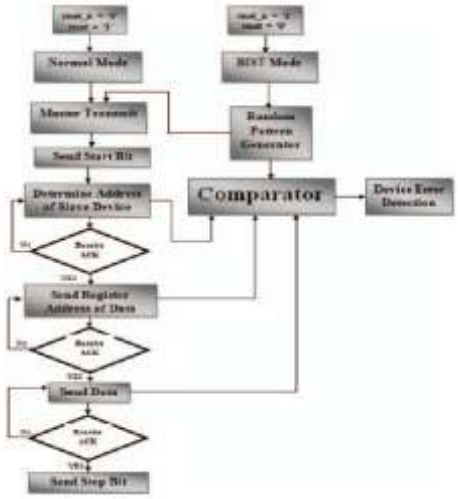


Fig -9. I2C Architecture with In-Built BIST

Authors have come up with more reliable, more even and tightly optimized version of the I2C by configuring the proposed architecture using Verilog HDL and it is also prototyped using Spartan series FPGA.

The application of BIST is extended to generate required thermal environment for thermal aware testing of FPGA by using own (FPGA) resources for controlling the heating elements, through [10]. This approach sidesteps use of any external component for heating FPGA devices, since they are integrated along the FPGA. Novelist presented binary techniques for BIST implementation and application-based testing. Authors have achieved wide range of chip temperature generation that is from 500 C to 1250 C on Virtex FPGA.

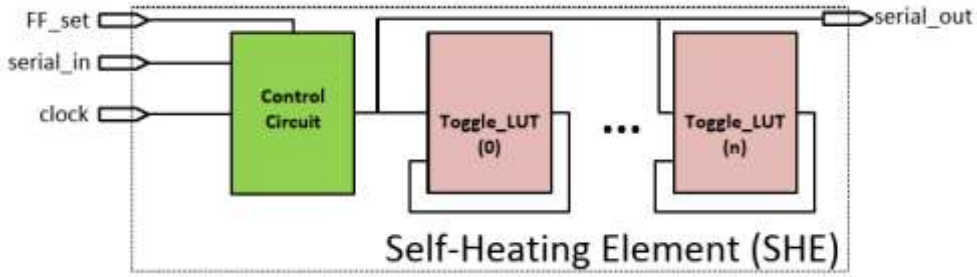


Fig -10. Self-Heating Components in The Said Design

Fault identification and analysis have the remarkable capability to advance the operational consistency and stability of manufacturing processes as the intention of fault identification and analysis are to reduce the manufacturing losses while making sure the protection of person and equipment. The authors [11] proposed an incorporated learning technique for mutually attaining fault identification and analysis of events in multivariate time series information. An autoencoder is used to identify rare faults and a long short-term network to categorize dissimilar kinds of faults. The training of the autoencoder is done manually, which is used for anomaly identification. To detect the kinds of faults the information acquired by the autoencoder is kept in a long short-term memory network. It mostly associates the strong low non-linear part of autoencoder for the rare fault identification and the strong series time learning capability of long short-term memory for the fault analysis.

The improvement in integrated circuits technologies guides the widespread utilization of memories and buffers in memory demanding applications. Hence, there is a threat of occurrence of the error in each fetch and write procedure. This paper proposed a mixed memory testing technique for static random-access memory by

combining two traditional testing algorithms. The main objective of the proposed work is to extract the best features of the proposed traditional testing algorithms and examine parameters like region utilization, error identification and diagnosis speed and power utilization, and error coverage. The authors [12] targeted stuck open errors, transition errors, stuck at errors, coupling errors, and data retention errors. The simulation outputs show that the proposed mixed memory testing technique gives efficiency up to 98% as it is unable to identify several coupling errors and data retention errors.

Static random-access memory plays an important role in processors. To fulfill the necessity of growing performance and power utilization, there is a need to designing of low voltage static random-access memory. In this paper, the authors proposed a new built-in self-test approach for testing low voltage static random-access memory. The proposed approach [13] is the enhancement version of the traditional March algorithm, which combines the uninterrupted write 0 and 1 operations. The proposed approach is realized by the user classify approach of Mentor tools. The proposed approach attained high error identification than the conventional March algorithm. To authenticate the accuracy of the proposed approach, a low voltage static random access memory chip is implemented and tested based on a complementary metal-oxide semiconductor procedure.

Memory dependability plays an essential role for the system on chips. Processor's memories are rising speedily to a huge amount in stipulations of dimension and concentration. As they require multifaceted design architectures, the occurrence ratio of manufacturing faults becomes progressively higher. There are two types of memories as volatile memories and non-volatile memories. The volatile memories need an electrical power supply to preserve the stored information, whereas the non-volatile memories do not need any power supply to preserve the stored information. When dealing with volatile and non-volatile memories, the fault identification and diagnosis techniques can be different. In this paper, the authors proposed an effective testing technology for the identification and diagnosis of errors or faults in volatile and non-volatile memories. [14]

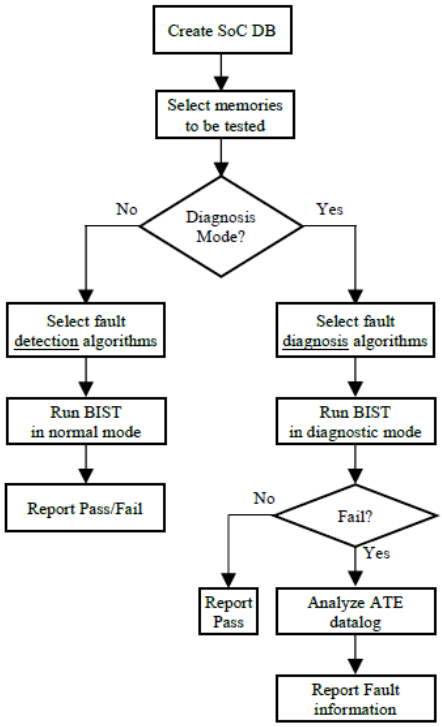


Fig -11 Fault identification and diagnosis flow

The focus of conventional spaceship design is on function execution, but not concentrate on self-testability. Self-testing of spaceship mainly depends on telemetry and instructions. The conventional built-in self-test technique is not well suited for spaceship architecture because its testing cost is very high, performance effectiveness is low and the test cycle is long. A novel built-in self-test technique for airspace has been proposed to find on-chip fault and diagnose it. The proposed technique is capable of providing speedy safeguarding and efficient reconfiguration. To improve the potential of spaceship quick assessment, the spaceship built-in self-test systems are intended from two characteristics of performance system and organization system. [15]

With the technical enhancement, the requirement for calculating power increases for the speedy performance of the memories. This again increases the demand for additional integrated circuits being committed to memories. In such conditions, the accurate fault testing of static random-access memories is a complex job. One of the most efficient fault testing techniques is an integrated memory built-in self-test but it consumes more area of the circuits. The present paper [16] proposed the implementation of a configurable built-in self-test technique single point and double point memory's fault testing. To authenticate the efficiency of the proposed algorithms, the improved testing environment with the memory module and error inoculation ability is employed.

To improve error identification probability in a particular time framework, judgments have to be taken in the path of choosing a subset of test cases from the entire set of accessible test cases. The authors proposed a quadratic programming methodology concern in the software testing field. The authors [17] concentrated on a precise difficulty to increase of probability of finding possible deficiencies. The proposed technique is best suited for medium to large category schemes wherein the worst-case situations the memory space complication of this technique does not go beyond the order of Gigabytes. The quadratic dynamic minimization technique is offered in an imitation code manner along with the active programming repetition procedure and possible assortment standard.

Memory which is a type of integrated circuit, employed in high dependability domains like aerospace, the defects of elements should be rapidly identified, finding the reason of defects to stay away from a bigger loss. According to the memory defects performance, the diagnosis algorithm must be implemented to precisely situate the fault position and differentiate the fault manner quickly. The design technique of the test algorithm for error analysis is proposed based on static random access memory failure diagnosis. The present paper evaluates the correlation between the fault manner of memory and the components of the test algorithm, in addition to the relative among the physical failure and the performance of the function failure. [18]

Memory distribution plays an essential part and has a great impact on the performance of the Parallel recursive brute force algorithm, as it requires high memory for information storage. In the paper [19] the authors proposed a modern realization of the Parallel recursive brute force algorithm that employed the static memory distribution method in place of the dynamic distribution method. Such arrangement is necessary to prevent memory organization expenses and mass conflict difficulties related to the dynamic memory distribution method. The authors used the Motif searching problem, which is recognized for the computationally concentrated problem. The required memory size is based on the complex size of the Motif searching problem which makes it tedious to utilize static memory distribution.

Resistive random-access memory is a rising non-volatile storage technology that has minimum write time, large resistance proportion with high and low resistance states, and low power utilization. 3-dimensional complementary metal oxide semiconductor structure consists of arrays of two end resistors between the CMOS subsystem and crossbar. The complementary metal-oxide molecular structure which can ease the power utilization in single resistor crossbars is utilized as a large-scale memory circuit. The authors examined the

electrical deficiencies in a Complementary metal oxide molecular structure together with a bridge. To diagnose the identified electrical deficiencies in CMOL structure, A parallel March fault test algorithm is proposed. [20]

CONCLUSIONS

After going through the detailed analysis of the studies proposed by the authors in connection to the Memory Self testing mechanism, it is observed that, effective work is done using diverse tools available for simulation, synthesis and for tight optimization as well. Few of the authors have also taken efforts to develop highly optimized generation of memory testing by considering significant factors like Power Utilization, Area Consumed, Speed of fault diagnosis and Number of Gate utilization. In the forthcoming paper, novel approach for development of Memory Testing will be discussed.

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