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A LOW POWER PIPELINE ADC WITH BACKGROUND CALIBRATION & DIGITAL CORRECTION

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Abstract-

This paper relates to low power pipeline analog to digital convertor with background calibration and digital correction. The pipeline ADC accomplishes this by a major reduction in the amount of circuitry required in the conversion process. Digital error correction logic and Flash ADC are integrated to form 10-bit pipelined ADC. Op-amp sharing technique have been used to minimize the power consumption in the pipelined ADCs. The power can also be saved by using charge distribution type dynamic comparator which is suitable for pipelined ADC. In the proposed ADC background calibration circuit comprises of a flash type ADC to summon up the data that is the difference in the MDAC requiring the digital error correction to provide a controlled yet comparable output which consumes 182.28 µW per flash ADC.

Keywords— Pipeline ADC, low power, pipeline, op-amp

INTRODUCTION

Analog to Digital Converters (ADCs) are used to generate a sequence of digital codes representing the strength of an input signal at corresponding time instants. A pipeline ADC is a type of ADC which contains a sequence of (pipeline) stages, with each stage resolving a number of bits forming a sub-code. The sub-codes generated by various stages are used to generate a digital code corresponding to the analog input sampled by the ADC.

The Pipeline ADC is use for converting medium to high speed and resolution with fast conversion rate. A pipeline stage comprises of sample and hold circuit, analog-to-digital converter (ADC) and digital-to-analog converter (DAC). The first stage converts the most significant bits (MSB) and the subsequent stages convert less significant bits until the least significant bits (LSB) are converted. There are several identical stages in pipeline ADC.

As in terms of power and speed performances, the pipeline architecture is considered as the most interesting one compared to other converter topologies in the communication applications. In the pipeline ADC, arrangement consists in placing several stages in cascade of low bit resolution per stage, and thus very fast. Typically this resolution is 1.5 or 2.5 bit stage. The ith stage provides two outputs; the first is a coarse resolution digital representation of the input while the second represents. All the stages are synchronized by the same clock. Once the first stage has produced and the second stage will start to quantify while the first one processes the next sample of the input.

Each stage (except the last stage) of a pipeline ADC generates a residue signal which is the difference of the input signal and the analog equivalent of the sub-code, the residual signal representing that portion of the input signal that needs to be resolved by subsequent stages. The residue signal represents a difference of the voltage of the input signal to the stage and the voltage value corresponding to the sub-code provided by the stage. The residue signal of one stage is provided as an input signal to the next stage in the sequence.

PIPELINE ADC ARCHITECTURE

Among various ADC architectures, pipelined ADC has the attractive feature of maintaining high accuracy at high conversion rate with low complexity and power consumption. It includes several cascaded stages. In each stage, there is a sample and hold (S/H) block, a sub-ADC, a sub-DAC, a subtractor and an inter-stage gain amplifier. The sampled input signal is first quantized by the sub-ADC to produce the output digital code for this stage. Then the output digital code is converted back to an analog signal by the sub-DAC. This quantized analog signal is subtracted from the input signal, resulting in a residue that is amplified and then passed onto the next stage.

The overall resolution of the pipelined ADC is the sum of the number of bits resolved in each stage and the throughput rate of the overall pipelined ADC is equal to each stage's throughput rate because of the pipelining technique. Figure below shows the generalized pipelined ADC architecture.

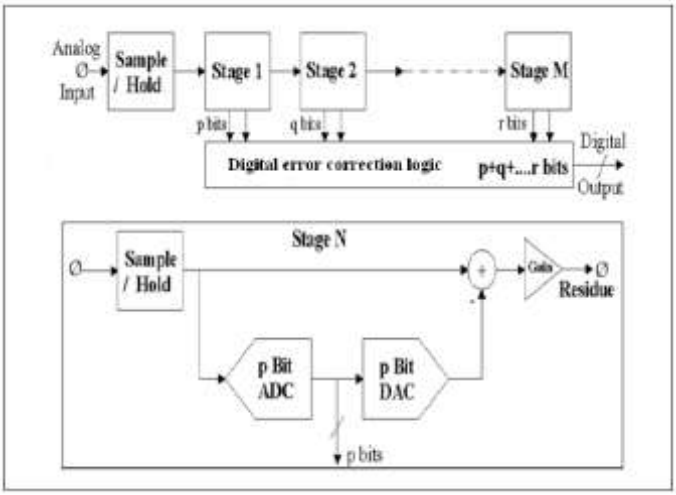

Fig. 1. Generalized pipelined ADC architecture

2.1 Sample and hold circuit

A sample and hold circuit is an analog device that samples (captures, takes) the voltage of a continuously varying analog signal and holds its value at a constant level for a specified minimum period of time. Sample and hold circuit is an important analog building block in many applications. Sample and hold circuits are used in analog-to-digital converters to eliminate variations in input signal that can corrupt the conversion process. The schematic of sample and hold circuit is shown in Fig. 2

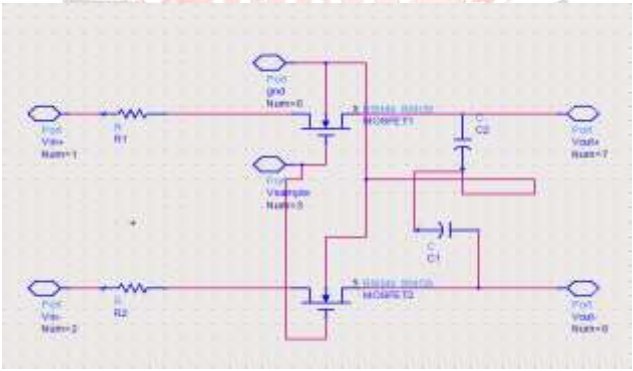

Fig. 2. Sample and hold circuit

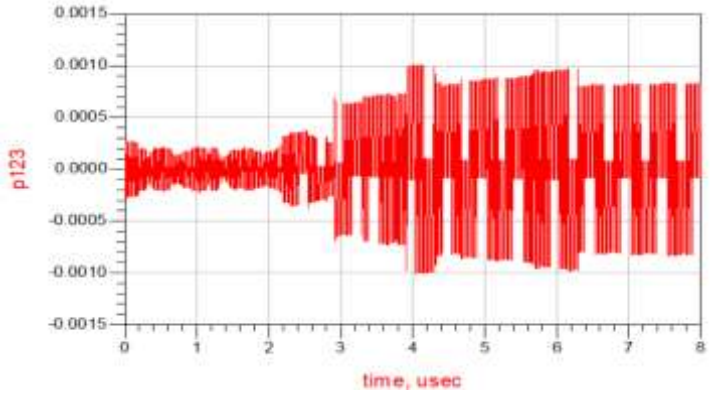

Fig. 3. Settling time of fully differential sample and hold circuit

Fig. 3 shows the settling time of sample and hold circuit. The settling time is obtained as 3.367 µs – 3.400 µs. So settling time is 0.2µs for the designed fully differential sample and hold circuit. The circuit consumes a power of 10µW.

2.2 Charge distribution type dynamic comparator

High-speed, low-power, small area requirement, and high resolution are the vital factors for designing high-speed, low-power applications ADC's. Hence comparator plays crucial role in designing low-power pipeline ADC. The power saving can be done by using simple dynamic comparator in low resolution flash A/D converter instead of using a pre-amplifier comparator. Fig. 4 shows the charge distribution dynamic comparator.

The sub-ADC in each 1.5 bits per stage consists of two fully differential comparators. Sub-ADC used is an important component of the pipelined stage. A 2 bits per stage flash ADC consists of 3 comparators. In 1.5 bits per pipeline stage, there are two comparators. One generates a threshold voltage +Vref /4 and other generates a threshold voltage of -Vref /4.

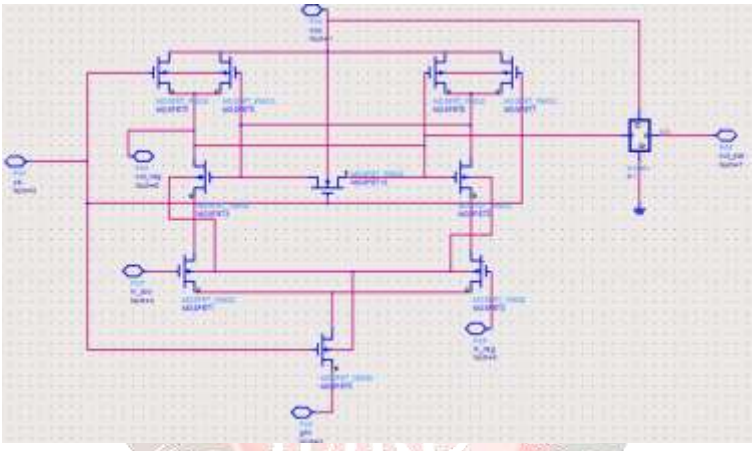

Fig. 4. Charge distribution dynamic comparator

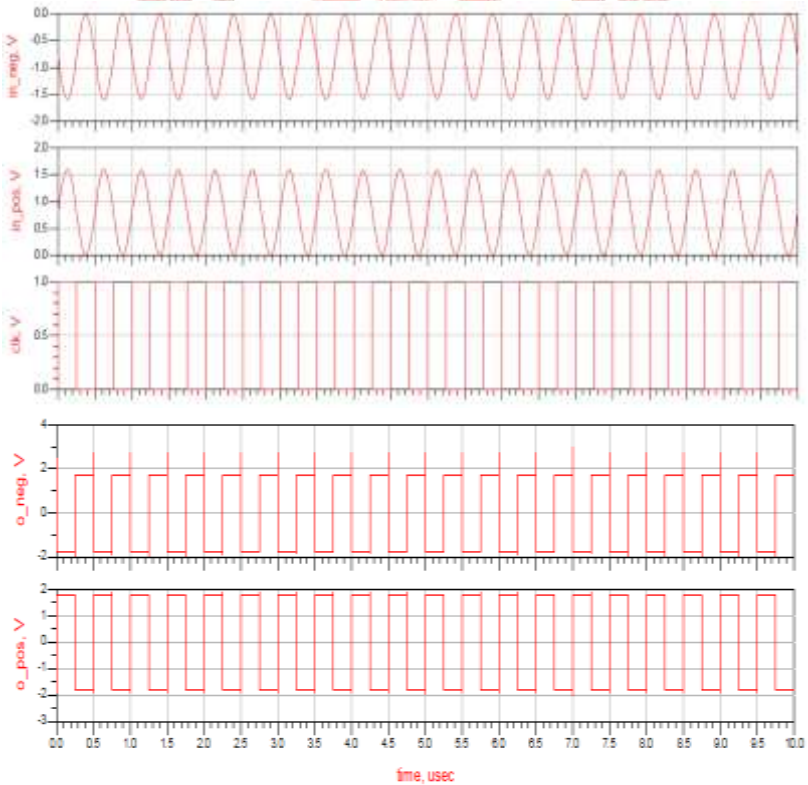

Fig. 5. Transient response of dynamic comparator

Fig. 5 shows the transient response of dynamic comparator. The inputs given to the comparator are analog in nature which is of 1.5Vpp. The comparator compares the two inputs and if the positive input is greater than the negative input the output becomes logic 1otherwise it becomes logic 0.

2.4 Op-amp sharing MDAC stage

The schematic of the op-amp sharing MDAC is shown in Fig. 6. Since the op-amp is used for both the stages, power consumption can be reduced to a certain limit. If one op-amp is shared between two successive stages the power consumption of the pipelined ADC is significantly reduced. Also the cross talk can be reduced by the introduction of additional switches. The power output obtained for the MDAC stage is 252 µw.

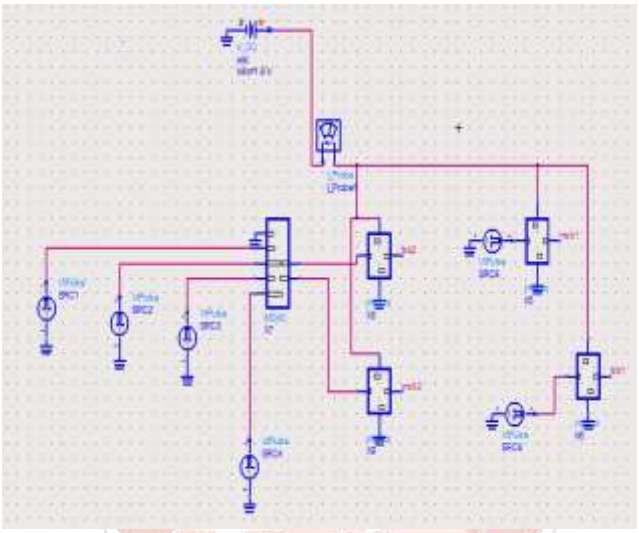

Fig 6. Schematic of op-amp sharing MDAC

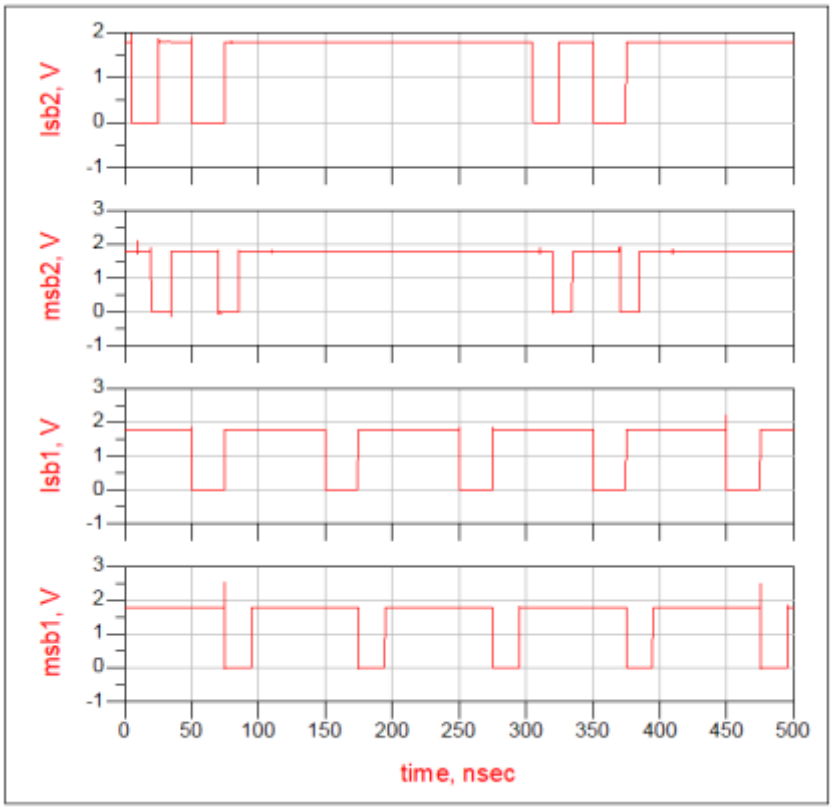

Fig. 7. Waveform of op-amp sharing MDAC

time	power	pavg
0.0000 sec	1.205E-10	2.520E-4
10.00 psec	8.630E-12	
20.00 psec	7.520E-11	
34.30 psec	5.905E-11	
49.53 psec	6.875E-11	
61.38 psec	6.039E-11	
84.89 psec	6.859E-11	
121.3 psec	6.030E-11	
188.9 psec	6.862E-11	
358.9 psec	6.024E-11	
730.6 psec	6.854E-11	
1.620 nsec	6.002E-11	
2.620 nsec	6.821E-11	
3.620 nsec	5.967E-11	
4.620 nsec	6.787E-11	
5.000 nsec	5.943E-11	
5.009 nsec	0.001	
5.015 nsec	3.602E-4	
5.021 nsec	2.533E-4	
5.027 nsec	4.882E-4	
5.034 nsec	2.161E-4	
5.052 nsec	4.771E-4	
5.074 nsec	3.107E-4	
5.106 nsec	3.901E-4	
5.145 nsec	3.396E-4	
5.189 nsec	3.763E-4	
5.287 nsec	3.489E-4	
5.468 nsec	3.672E-4	
5.978 nsec	3.561E-4	
6.848 nsec	3.623E-4	

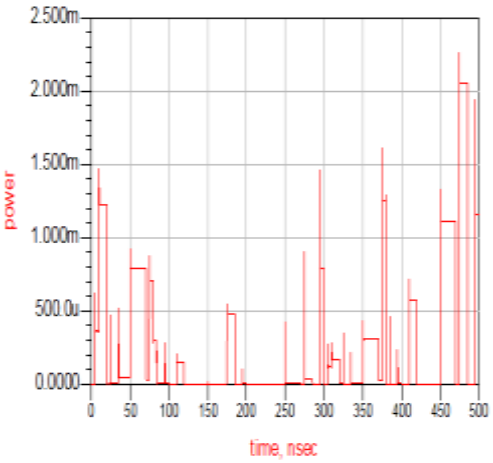

Fig. 8. Power consumption obtained for op-amp sharing MDAC

BACKGROUND CALIBRATION AND DIGITAL CORRECTION

Background calibration circuit comprises of a flash type ADC to summon up the data that is the difference in the MDAC requiring the digital error correction to provide a controlled yet comparable output. Digital error correction logic circuit is mainly used for eliminating the offset error from sub sequent stages in a pipeline ADC. If sub sequent stages detect an error, this error is digitally eliminated by adding or subtracting the bits from the digital bits.

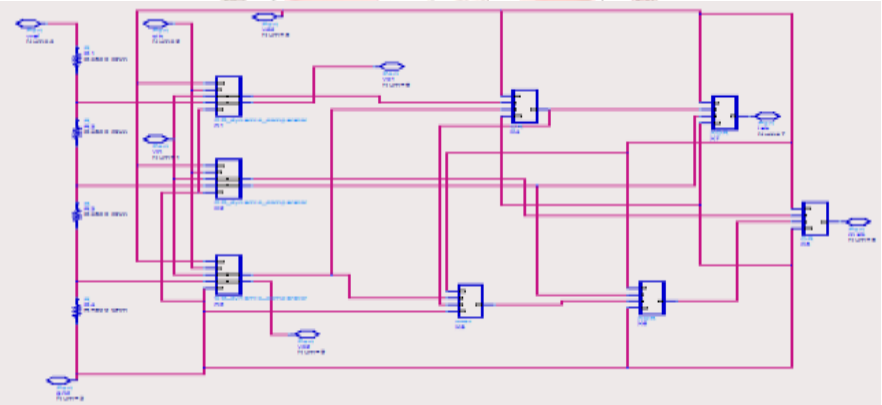

Fig. 9. Background calibration circuit

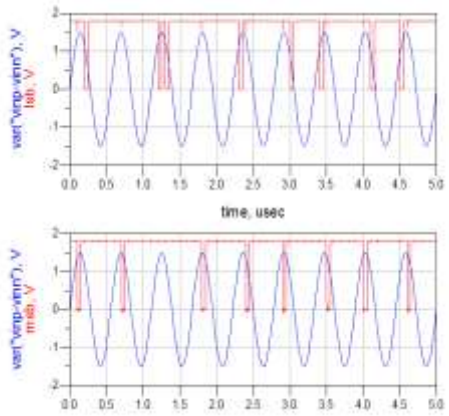

Fig. 10. Output waveform of Background calibration circuit with average power of 182.28µW

Performance Summary of Background Calibration Circuit

Parameter	Values
Technology(nm)	45
Resolution(bits)	2 bits per flash type
Power	182.28 µW per flash adc
Calibration	Background

CONCLUSION

The pipelined ADC employs background calibration and digital correction for power reduction. The sub circuits of various stages were integrated to form the single bit stage which was then cascaded to form the 10-bit pipelined ADC. Dynamic comparator is also designed and the same is used to build sub-ADC's which generates the LSB and MSB of each single stage. The designed pipeline ADC can be used in various applications such as data acquisition systems, wireless receiver, base station, digital video, cable modem and fast Ethernet.

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