

2D MESH TOPOLOGY USING ROUTING ALGORITHMS FOR NOC ARCHITECTURE

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ABSTRACT-

As per the recent studies, the development of integration technology, System on-Chip (SoC), has large number of transistor. As the microprocessor industry is moving from single-core to multicore architectures, which require efficient communications processors. Also both SoC and microprocessor are used for a high-performance, flexible, scalable, and design-friendly interconnection. Interconnection architectures are usually based on dedicated wires or shared buses. NoC has been proposed as a highly structured and scalable solution to address communication problems in SoC. Onchip interconnection network provides advantages over dedicated wiring and buses, i.e. high-bandwidth, low-latency, low-power consumption and scalability. Among these topologies, mesh topology has gained more consideration by designers due to its simplicity. In this paper, we compare source routing algorithm and junction based routing algorithm using 2D mesh topology of NoC architecture in terms of different performance metrics such as, latency, power consumption, and power/throughput ratio.

Index Terms— NoC, 2D mesh topology, Routing algorithms, Junction-based routing, VBR traffic, simulator.

INTRODUCTION

NoC has been proposed as a highly structured and scalable solution to address communication problems in SoC. The main features of NoC platforms are routing algorithm and topology. The NoC parameters are used to gives better performance of the system as compared to SoC. For evaluating NoC using a simulator, data is transmitted into the network in different ways and performance values are evaluated regarding the traffic. Number of messages is transported back and forth via the interconnection networks. Thus, the interconnections among multiple cores on a chip have a significant impact on communication and performance of the chip design in terms of end-to-end delay, throughput, and packets loss ratio. Source routing has an important disadvantage of overhead for storing the path Information in header of each packet sent. This disadvantage becomes worse as the size of the network grows. The Junction Based Routing (JBR) can be used to remove this disadvantage. The idea of junction based routing is basically derived from the railway networks.

LITERATURE REVIEW

This section discusses the results obtained from the previous researches: N.Ashokkumar, Nagarajan, S.Ravanaraja proposed that, Network-on-chip is a very active research field with many practical applications in industry. Based on

the study, they identified as especially crucial for continued development and success of NoC paradigm as procedures and test cases for benchmarking, traffic characterization and modeling, design automation, latency and power minimization, fault-tolerance, QoS policies, prototyping, and network interface design.[1]

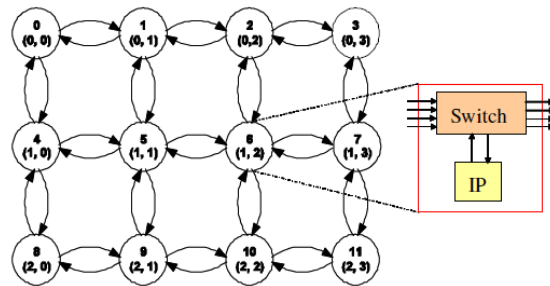
Nikolay Kavaldjiev, Gerard J. M. Smit, Pascal T. Wolkotte, Pierre G. Jansen described possibilities of providing throughput guarantees in a network-on-chip by appropriate traffic routing. A source routing function is used to find routes with specified throughput for the data streams in a streaming multiprocessor system-on-chip. Thus the result for throughput guarantees to streaming traffic is feasible. Therefore, they conclude that mapping algorithm is of greater importance for the system performance than the routing algorithm and it is profitable to use a more complex mapping algorithm that preserves the communication locality together with a simple routing algorithm.

Saad Mubeen and Shashi Kumar described very important for exploiting enormous computing power available on a multicore chip. Routing algorithms significantly affect the performance of a NoC. Most of the existing NoC architectural proposals advocate distributed routing algorithms for building NoC platforms. Although source routing offers many advantages, but researchers avoided it due to its apparent disadvantage of larger header size requirement that results in lower bandwidth utilization. The simulation results that 28% lower latency even at medium load, as compared to distributed routing. Also designed a router to support source routing for mesh topology NoC platforms. A Matlab based tool called MatPC has been developed for this purpose. From this, the use of source routing in mesh topology NoC, because of the small and fixed size of practical NoCs, the overhead of source routing is negligible and it is easily compensated by a large number of its advantages, including lower router cost and higher communication speed of the router. Evaluation results show that source routing gives higher latency and throughput performance as compared to corresponding distributed routing. [3]

Fahimeh Jafari, Axel Jantsch, and Zhonghai Lu, proposed that aggregate scheduling in routers merges several flows into one aggregate flow. They proposed an approach for computing the end-to-end delay bound of individual flows in a FIFO multiplexer under aggregate scheduling. A synthetic case study exhibits that the end-to-end delay bound is up to 33.6% tighter than the case without considering the traffic peak behavior. They presented and proved the required propositions for computing delay bound of VBR flows in a FIFO multiplexing network. The propositions can be applied for an architecture based on aggregate scheduling. [4]

Network topology provides the interconnection of various elements (links, nodes, etc.) of a network. Design of NoC router architecture depends upon the network topology. The mesh topology is one of the most common network topologies to use.

Two-dimensional mesh topology will be used throughout in this. It is one of the easiest topologies to implement on a silicon die, because of its flat configuration. A mesh-shaped network consists of m columns and n rows. The routers are situated in the intersections of two wires and the computational resources are near routers. Addresses of routers and resources can be easily defined as x - y coordinates in mesh. Mesh topology is easy to implement as all nodes are in equally distance as shown in Figure:



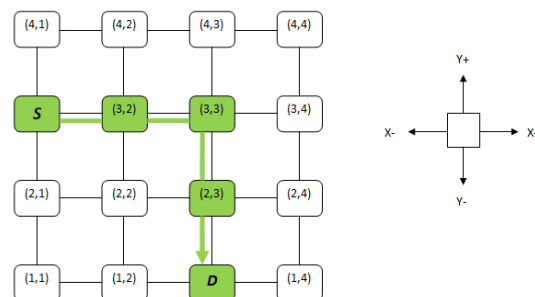
It is one of the easiest topologies to implement on a silicon die, because of its flat configuration. Mesh size given as $R \times C$ means the number of node rows is R and the number of node columns is C . Cube and hypercube are also regular topologies similar to mesh.

ROUTING ALGORITHM

Routing algorithms define the path taken by a packet between source and target switches. They must prevent deadlock, livelock, and starvation [8][9] situations. Deadlock may be defined as a cyclic dependency among nodes requiring access to a set of resources, so that no forward progress can be made, no matter what sequence of events happens [6]. Livelock refers to packets circulating the network without ever making any progress towards their destination. Starvation happens when a packet in a buffer requests an output channel, being blocked because the output channel is always allocated to another packet. Routing algorithms can be classified according to the three different criteria: (i) where the routing decisions are taken; (ii) how a path is defined, and (iii) the path length. In source routing, the whole path is decided at the source switch, the header of the packet has to carry all the routing information, increasing the packet size [9].

I. X-Y Routing algorithm

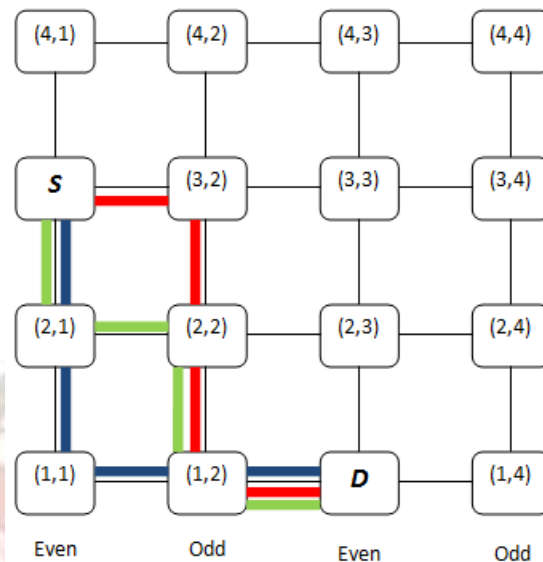
In X-Y routing, if the column of the source and the column of the destination are different, a packet moves along the horizontal axis toward the destination. After that it makes progress to the destination vertically. In Figure, source node (3,1) is communicating with (1,3). The path which is shown using the vector is allowed for sending data from S to D .



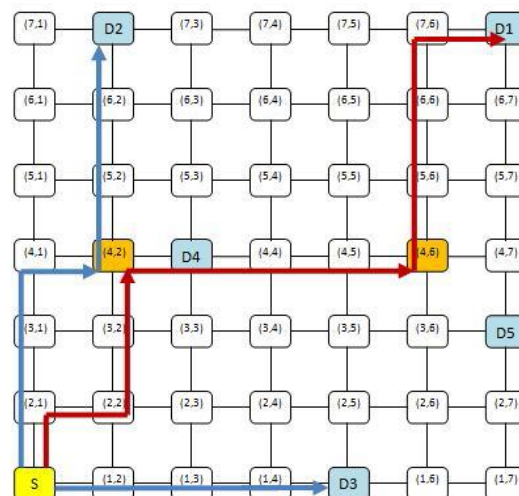
Allowed path in XY routing algorithm.

II. OE Routing Algorithm

Odd-Even routing algorithm is another partially adaptive routing algorithm and has a higher adaptiveness in compared with the other routing algorithms [3][7]. Packets are not allowed to make an East-North or East-South turn at the nodes that are in an even column of a mesh network. North-West or South-West turn is limited at the nodes that are in an odd column. For instance, source node S is sending data to destination node D. Applying Odd-Even routing algorithm, there are three possible paths for sending data from S to D that are depicted in Figure:



Junction-Based Routing Source routing has an important disadvantage of overhead for storing the path information in header of each packet sent. This disadvantage becomes worse as the size of the network grows. In this chapter we describe a routing technique, called Junction Based Routing (JBR) to remove this disadvantage. The idea of junction based routing is basically derived from the railway networks. Railway networks generally have a few large stations, called junctions which are connected by fast railways. A long distance journeys from a small town to another small town is achieved by first going to the nearest junction close to the source and from there reaching a junction close to the destination. Consider the following 7x7 mesh topology NoC that has the diameter of 13 hops



The node that is presented using (x,y) is located at x th row and y th column. Distance between nodes that is located at position (x_1,y_1) and (x_2,y_2) is calculated using the formula:

Distance = $|y_2-y_1| + |x_2-x_1|$. The number of routers used from a source node to a destination node is equal to the number of links used plus one. We define hop count as number of routers on the path from a source to the destination.

Hop Count = Distance + 1.

III. VARIABLE BIT RATE

The VBR service category is used for connections that transport traffic at variable rates traffic that relies on accurate timing between the traffic source and destination. An example of traffic that requires this type of service category are variable rate, compressed video streams. Sources that use VBR connections are expected to transmit at a rate that varies with time (for example, traffic that can be considered bursty). VBR connections can be characterized by a Peak Cell Rate (PCR), Sustained Cell Rate (SCR), and Maximum Burst Size (MBS).

IV. PERFORMANCE PARAMETERS

Some of the most important parameters that are used in evaluating the performance of NoCs are defined in this subsection briefly.

Latency

Network latency presents the required time to transfer n bytes of payload from its source to its destination. Latency consists of routing delay, contention delay, channel occupancy and overhead.

Bandwidth

Communication bandwidth is the amount of data that can be moved using a communication link in a unit time period.

Throughput

Throughput is the total number of received packets by the destinations per time unit.

Packet Loss

Packet loss happens when one or more packets do not reach their destination due to the error introduced by the network, the contention for network link or lack of buffer space etc.

I. CONCLUSION

In this research we design the 2D 7x7 mesh topology under the VBR traffic using Junction Based Routing algorithm. Junction Based Routing algorithm gives path information for only a few hops is stored in the packet header. With this information, the packet reaches the destination, or reaches a junction from where the path information for on-ward path is picked up. Also by using this algorithm latency does not increase so much using junctions. Throughput also does not level off significantly. Header flit in JBR can carry payload data and this improves the performance of JBR in terms of throughput and latency compared to source routing which needs to store large path information.

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