AN EFFICIENT FAULT TOLERANT IIR FILTERS BASED ON ERROR CORRECTION CODES

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ABSTRACT-

Filters are broadly used in dealing out with signal processing and communication systems. The filters so used are digital filters. In those systems, accuracy to efficient operation of signal are insignificant and that is why implementation of fault tolerant filters are needed. Over the duration, lots of techniques that make use of the filters structure and properties to achieve fault tolerance have been proposed. Enhancing technology makes system more complex that include many filters. In those complex systems, it is frequent to have number of filters in circuit that functions in parallel architecture. In parallel combination of filters there apply the same filter to different input signals. In recent times researcher has projected, a simple technique having the existence of parallel filters to accomplish fault tolerance. So, from this case study the idea to implement parallel filters and digitally correct the errors are generalized. It has been proposed to protect digital circuits in signal processing by single error detecting codes and single error correcting codes. This scheme permits extra efficient protection in presence of large number of parallel filters. The technique has evaluated using study on parallel infinite impulse response filters making effectiveness in terms of protection and implementation cost. The enhanced hase BCH decoder is designed using hardware description language called Verilog and synthesized in Xilinx ISE 13.2.

Keywords— Error correction codes (ECCs), BCH Codes, Syndrome Block, filters, errors.

I. INTRODUCTION

Filters are often used in electronic systems to emphasize signals in certain frequency ranges and reject signals in other frequency ranges. In circuit theory, a filter is an electrical network that alters the amplitude and/or phase characteristics of a signal with respect to frequency. Ideally, a filter will not add new frequencies to the input signal, nor will it change the component frequencies of that signal, but it will change the relative amplitudes of the various frequency components and/or their phase relationships. Filters of some sort are essential in the operation of most electronic circuits. As the behavioural properties of signal changes the techniques of filtering it will be differ the types of filter used. Being specific with the types of filter, the digital filters have vast applications in digital signal processing. Filtering is also a class of signal processing, the defining feature of filters being the complete or partial suppression of some aspect of the signal. Today filters are widely used in number of application circuitry which based on automotive, medical, and space where reliability of performance in digital electronic circuits is critical. In signal processing, a digital filter is a device or process that removes some unwanted component or feature from a signal. Digital filters are used for two general purposes; separation of signals that have been combined, and restoration of signals that have been distorted in some way. Digital filters are very important part of DSP. In fact, their extraordinary performance is one of the key reasons that DSP has become so popular. It is common in DSP to say that a filter's input and output signals are in the time domain. This is because signals are usually created by sampling at regular intervals of time. As the applications of digital circuits in signal processing got advanced, possibilities of faults have increased and its detection and correction within digital circuitry also need to be enhanced.

II. CONCEPT OF FAULT TOLERANCE

A number of techniques can be used to protect a circuit from errors. Those range from modifications in the manufacturing process of the circuits to reduce the number of errors to adding redundancy at the logic or system level to ensure that errors do not affect the system functionality. Digital Filters are one of the most commonly used signal processing circuits and several techniques have been proposed to protect them from errors. There are number of methods used to identify faults and the actions necessary to correct the faults within circuit. Digital filters are widely used in signal processing and communication systems. There are different fault tolerance approaches to conventional computational circuits and the DSP circuits. In some cases, the reliability of those systems is critical, and fault tolerant filter implementations are needed. Over the years, many techniques that exploit the filters structure and properties to achieve fault tolerance have been proposed. In all the techniques mentioned so far, the protection of a single filter is considered. In recent times researcher has projected, a simple technique having the existence of parallel filters to accomplish fault tolerance [1]. It has been proposed to protect digital circuits in signal processing by single error detecting codes and single error correcting codes[14]. Filters can be protected using error correction codes (ECCs) in which each filter is the equivalent of a bit in a traditional ECC and filters are arranged in parallel architecture.

III. FILTER SPECIFICATIONS

FIR digital filters

A Finite Impulse Response (FIR) digital filter is one whose impulse response is of finite duration. A difference equation is the discrete time equivalent of a continuous time differential equation. The general difference equation for a FIR digital filter is

$$y(n) = \sum b_k x(n - k)$$

where y(n) is the filter output at discrete time instance n, bk is the k-th feed forward tap, or filter coefficient, and x(nk) is the filter input delayed by k samples. The ∑ denotes summation from $k = 0$ to $k = M - 1$ where M is the number of feed forward taps in the FIR filter.

IIR digital filters

Another type of digital filter is the Infinite Impulse Response (IIR) filter. As you may have guessed, the impulse response of an IIR filter is of infinite duration. Mathematically speaking, this means that either τ1 or τ2 in (1) is equal to ∞. The general difference equation for an IIR digital filter is

y□*n*□ □□ □ □∑ak y□*n* □ □*k*□ □□ □∑□bk x□*n* □ □*k*□

where ak is the *k*-th feedback tap. The left □∑ denotes summation from $k = 1$ to $k = N - 1$ where N is the number of feedback taps in the IIR filter. The right ∑ denotes summation from $k = 0$ to $k = M$B-1 where M is the number of feed forward taps.

IIR filters are useful for high-speed designs because they typically require a lower number of multiplies compared to

FIR filters. IIR filters can also be designed to have a frequency response that is a discrete version of the frequency response of an analog filter.

IV. EXISTING METHOD

FIR Filter with Error Correcting Hamming Codes

The existing technique is based on the use of the ECCs. A simple ECC takes a block of k bits and produces a block of n bits by adding $n-k$ parity check bits [14]. The parity check bits are XOR combinations of the k data bits. By properly designing those combinations it is possible to detect and correct errors. As an example, let us consider a simple Hamming code [13] with $k = 4$ and $n = 7$. In this case, the three parity check bits $p1$, $p2$, $p3$ are computed as a function of the data bits $d1$, $d2$, $d3$, $d4$ as follows:

$$p_1 = d_1 \oplus d_2 \oplus d_3$$
$$p_2 = d_1 \oplus d_2 \oplus d_4$$
$$p_3 = d_1 \oplus d_3 \oplus d_4.$$

The data and parity check bits are stored and can be recovered later even if there is an error in one of the bits. This is done by recomputing the parity check bits and comparing the results with the values stored. In the example considered, an error on $d1$ will cause errors on the three parity checks; an error on $d2$ only in $p1$ and $p2$; an error on $d3$ in $p1$ and $p3$; and finally an error on $d4$ in $p2$ and $p3$. Therefore, the data bit in error can be located and the error can be corrected. This is commonly formulated in terms of the generating G and parity check H matrixes.

$$G = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix}$$

$$H = \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix}$$

Encoding is done by computing $y = x \cdot G$ and error detection is done by computing $s = y \bullet HT$, where the operator • is based on module two addition (XOR) and multiplication[1][7]. Correction is done using the vector s, known as syndrome, to identify the bit in error.

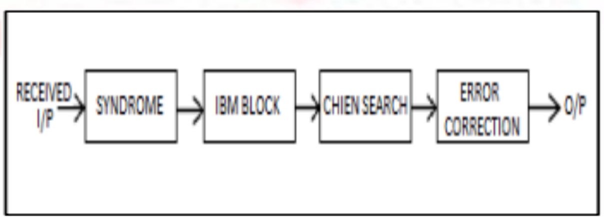
V. Problem Definition

The various types of techniques are verified, tested and implemented in digital signal processing circuits having parallel filters as the block to be protected. Digital filters are one of the most commonly used signal processing circuits and several techniques have been proposed to protect them from errors. Most of them have focused on finite-impulse response (FIR) filters. The proposed scheme [1] is based on the application of error correction codes (ECCs) using each of the filter outputs as the equivalent of a bit in and ECC codeword. This is more efficient implementations when the number of parallel filters is large.

As the existing scheme is more efficient only when the number of filters is large, it limits the area of application to the higher order when implemented using parallel FIR filters[9]. It makes considerable difference in cost when used for lower order application of DSP. Further, the scheme cannot be used to provide more powerful protection using advanced ECCs that can correct failures in multiples modules. Many properties such as symmetric filters satisfying the perfect reconstruction condition can only be obtained by IIR filter.

VI. Proposed scheme

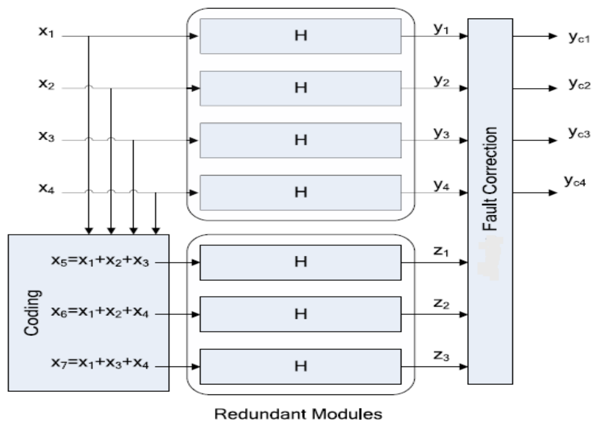
The new technique is also based on the use of the ECCs. The idea behind these codes is to add redundancy bits to the data being transmitted so that even if some errors occur due to noise in the channel, the data can be correctly received at the destination end. Bose, Ray- Chaudhuri, Hocquenghem (BCH) codes are one of the error-correcting codes. The BCH decoder consists of four blocks namely syndrome block, IBM block, chien search block and error correction block.



This paper describes a new method for error detection in syndrome and chien search block of BCH decoder. The proposed syndrome block is used to reduce the number of computation by calculating the even number syndromes from the corresponding odd number syndromes.

Redundant Module

Many communication channels are subjected to channel noise which introduces the errors during transmission of messages from the source to receiver [6]. The channel coding theory states that the reliable transmission is achievable by performing proper coding. “Channel Coding” is the technique, which is used to sustain the originality of the information bits, to avoid the retransmission of information bits as well as to detect and correct any error which has been occurred during transmission. Error detection is the detection of errors caused by noise or other impairments during transmission from the transmitter to the receiver. It uses the concept of redundancy [8], which means adding of extra bits for detecting errors at the destination. In error correction we used BCH decoder at receiver, which can automatically correct certain errors and enables reconstruction of the original data.



This ECC scheme can be applied to the parallel filters considered by defining a set of check filters z_j . For the case of four filters $y1$, $y2$, $y3$, $y4$ and the BCH code, the check filters would be

$$z_1[n] = \sum_{l=0}^{\infty} (x_1[n-l] + x_2[n-l] + x_3[n-l]) \cdot h[l]$$
$$z_2[n] = \sum_{l=0}^{\infty} (x_1[n-l] + x_2[n-l] + x_4[n-l]) \cdot h[l]$$
$$z_3[n] = \sum_{l=0}^{\infty} (x_1[n-l] + x_3[n-l] + x_4[n-l]) \cdot h[l]$$

For example, an error on filter $y1$ will cause errors on the checks of $z1$, $z2$, and $z3$. Similarly, errors on the other filters will cause errors on a different group of zi . Therefore, as with the traditional ECCs, the error can be located and corrected.

The first step at the decoding process is to store the received codeword in a buffer and then calculate the syndromes. The input to the syndrome module is the received codeword. The received polynomial may be corrupted with error pattern e(x)

r(x) = c(x) + e(x)

Where the received codeword is

$$r(x) = r_0 + r_1 x + \cdots . + r_{n-1} x^{n-1}$$

Transmitted codeword is given by

$$c_x = c_0 + c_1 + \cdots + c_{n-1} x^{n-1}$$

The error pattern is

$$e_x = e_0 + e_1 + \cdots + e_{n-1} x^{n-1}$$

Syndrome Si can be computed by :

$$s_i = r(\alpha^i) = r_0 + r_1 \alpha^i + r_2 \alpha^{2i} + r_3 \alpha^{3i} + \cdots + r_{n-1} \alpha^{(n-1)i}$$

where 1 ≤ i ≤ 2t – 1.

For BCH equation the three syndromes are:

$$s_1 = r(\alpha^1) = r_0 + r_1 \alpha^1 + r_2 \alpha^2 + r_3 \alpha^3 + \cdots + r_{n-1} \alpha^{62}$$

$$s_2 = r(\alpha^2) = r_0 + r_1 \alpha^2 + r_2 \alpha^4 + r_3 \alpha^6 + \cdots + r_{n-1} \alpha^{124}$$

$$s_3 = r(\alpha^2) = r_0 + r_1 \alpha^3 + r_2 \alpha^6 + r_3 \alpha^9 + \cdots + r_{n-1} \alpha^{186}$$

where α is the primitive element in GF(26) If there is no error in the received codeword then syndromes generated will be zero. Since the syndromes only depends on the error polynomial, and if the syndromes are nonzero then next step is to find out the coefficients of error locator polynomial.H code are as given below,

Block Length: $n = 2^m – 1$

Information Bits: $k = 2^m - m – 1$

Parity Check Bits: $n - k = mt$

Correctable Errors: $t = 1$

Minimum distance: dmin ≥ 2t + 1

These conditions are true for $m > 2$. For example, with $m = 4$, there are $n = 15$ total bits per block or codeword, $k = 11$ information bits, $n - k = 4$ parity check bits, and the code can correct $t = 1$ error.

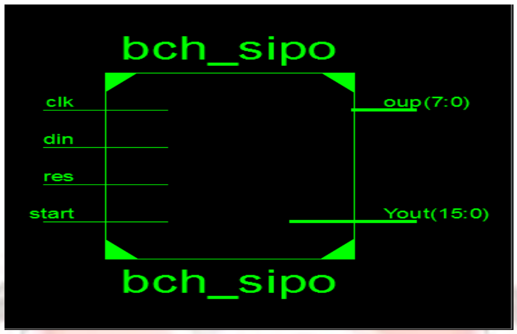
A representative codeword would be

100101001010010

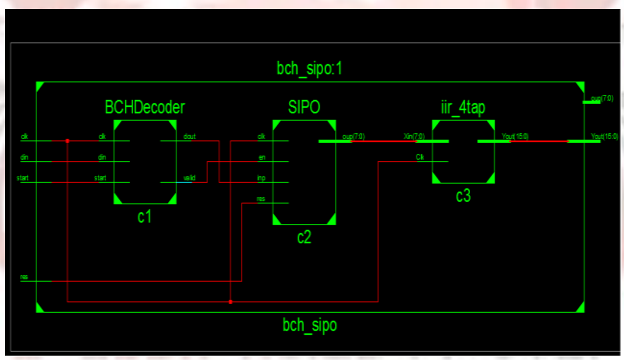
where the four bits on the right (0010) are the parity check bits. By choosing the value of *m*, we can create a single error correcting code that fits our block length and correction requirements. This one is customarily denoted a (15, 4) code, telling us the total number of bits in a codeword (15) and the number of information bits (4).

VII. SIMULATION RESULTS

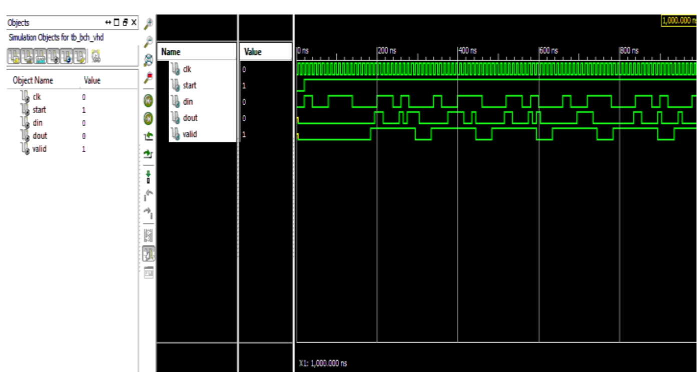
Simulation is carried out using Xilinx ISE 13.2 design suit tool.



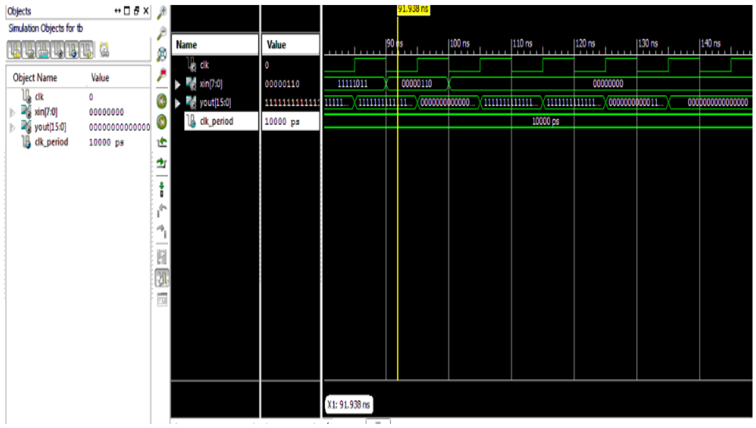
RTL Top view of BCH Decoder



RTL Schematic of internal blocks

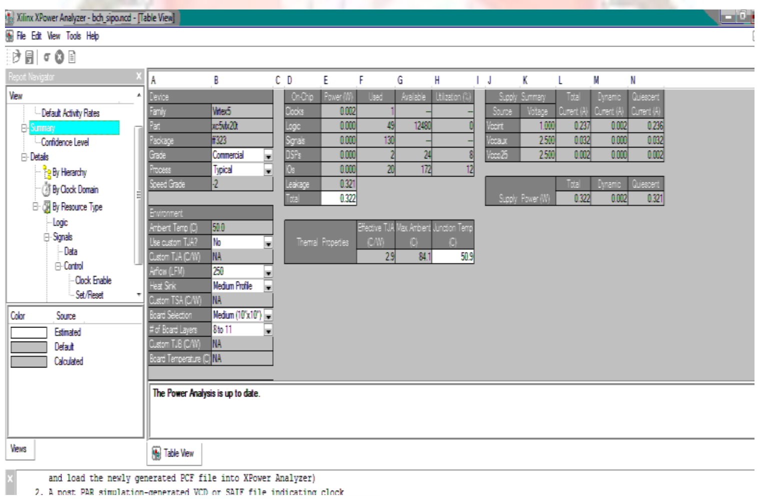


Simulation Result

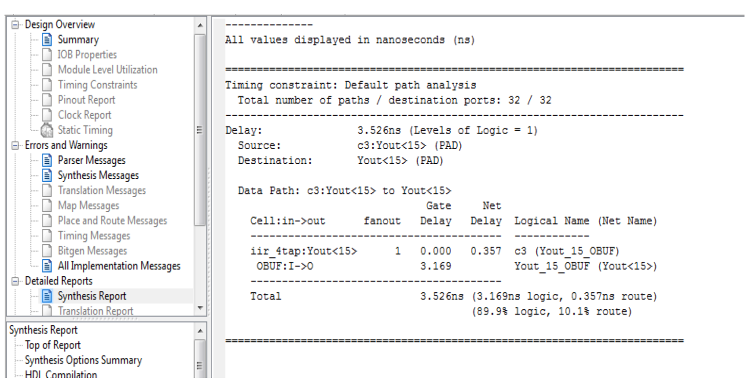


Output Simulation Test-bench Waveform

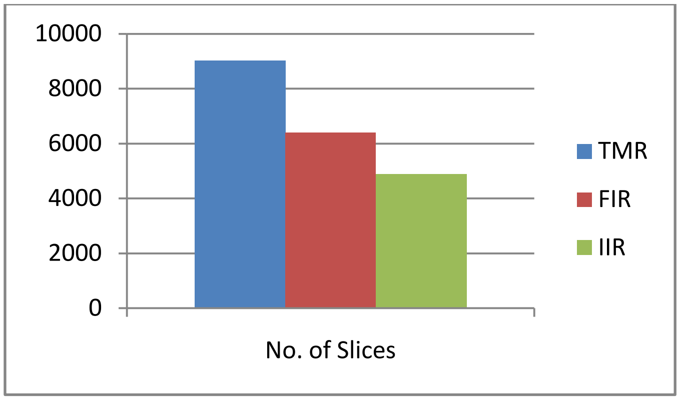
VIII. PERFORMANCE ANALYSIS

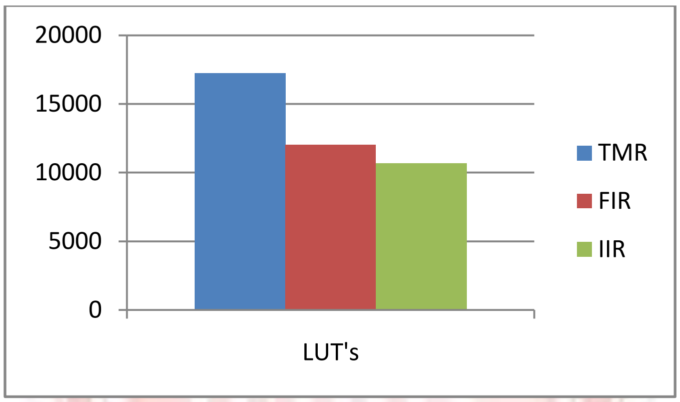


Power Analysis



Synthesis Report





VII. CONCLUSION

In this review paper a new scheme to protect parallel filters that are commonly found in modern signal processing circuits has presented. The approach is based on applying ECCs to the parallel filters outputs to detect and correct errors. The scheme can be used for parallel filters that have the same response and process different input signals. An objective has also been discussed to show the effectiveness of the scheme in terms of error correction and problem definition also shows the overheads. The proposed scheme can also make system cost lower. Proposed work will result in more efficient fault tolerant system using parallel IIR filters based on ECCs, which will meet the goal to achieve low power consumption, increase area of application and high speed.

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BIOGRAPHIES

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