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A SURVEY PAPER ON APPLICATION DEPENDENT ADDER SYSTEM

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ABSTRACT :

In high speed VLSI applications adders play important role. According to conventional studies much research is done on various parameters like speed, area, and power. Considering recent scenario optimization of all parameters is needed, this gives rise to idea of hybrid systems. Thus in this work two new hybrid carry select adders are studied involving the carry select and section carry based carry look ahead sub adders. Performance of proposed designs is studied under Verilog HDL. In this paper reconfigurable hybrid system is proposed involving three different adders delivering optimized area, power and delay individually according to user's application.

Keyword: Carry select adder, Reconfigurable, Verilog.

1. INTRODUCTION :

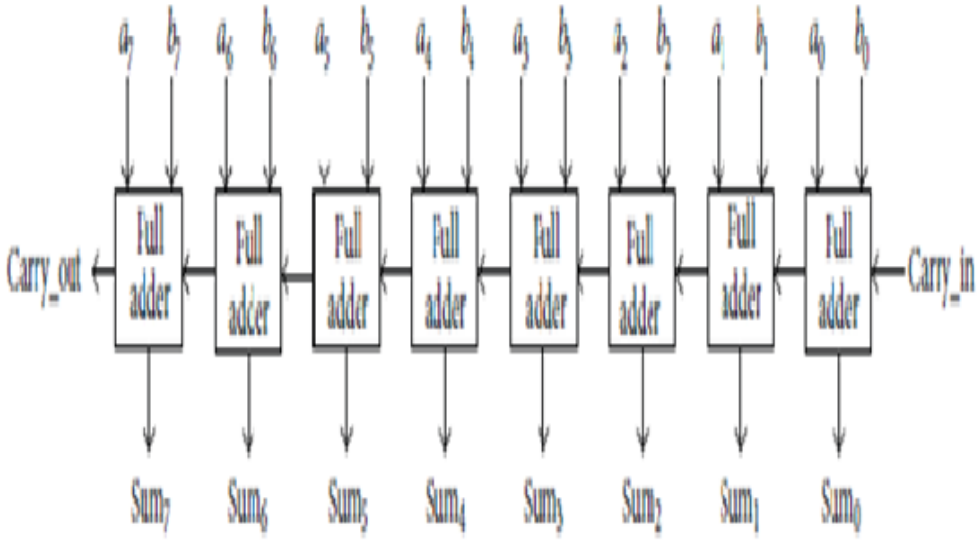
Adder is the basic building block of every arithmetic and logical operations. There are various types of adder already exist i.e Ripple carry adder(RCA),Carry look ahead adder(CLA),Carry select adder(CSLA),Carry save adder(CSA) and so on. So there is need to concentrate on the various performance parameter of adder such as speed, area, power and delay. Among all these adders CSLA provides the good compromise between low area occupancy of RCA and High speed performance of CLA. This is the only reason that we are focusing on CSLA. Also Carry select adder (CSLA) belongs to the family of high speed square-root time adders. Carry select adders are realized using the following:

a. Full adders and 2 : 1 multiplexers.
b. Full adders, binary to excess 1 code converters, and 2 : 1 multiplexers
c. Sharing of common Boolean logic.

Carry select adder is classified as Homogeneous and Heterogeneous CSLA. It has been widely implemented using the following topologies and computational elements:

a. Conventional CSLA
b. CSLA with Binary to excess converter. (BEC)
c. CSLA based on common Boolean logic (CBL) sharing
d. Hybrid CSLA and CLA structures
e. Hybrid CSLA and CLA including BECs

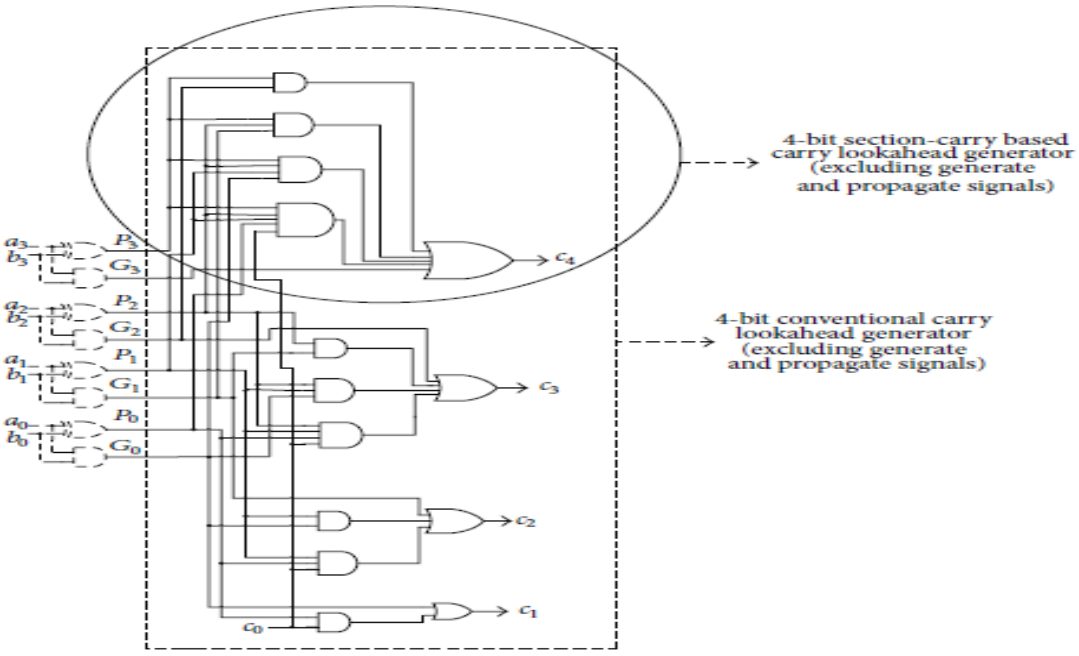
Ripple Carry Adder (RCA)



8- bit RCA [1]

- Multiple full adder circuit can be cascaded in parallel to add N-bit number. It is a logic circuit in which the carry out of each full adder is the carry in of the succeeding next full adder. As carry bits get rippled it is called as ripple carry adder. The carry generated from each full adder is given to next full adder and so on. Hence, the carry is propagated in a serial computation.
- Hence, delay is more as the number of bits is increased in RCA.

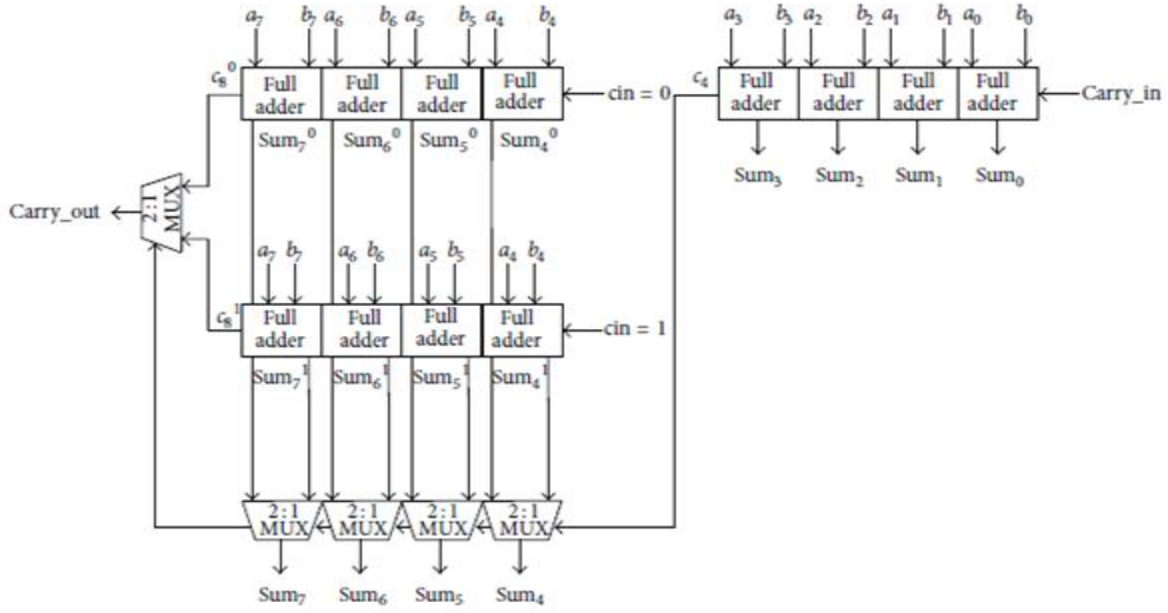
Carry Look Ahead Adder (CLA)



(a) 4-Bit Conventional & Section Carry Based Carry Look ahead Adder[1]

- Carry look ahead adder solves the carry delay problem by calculating the carry signals in advance based on input signal. Therefore CLA is faster than RCA.
- Carry look ahead adder reduces the carry delay by reducing the number of gates through which a carry signal must propagate in the generation and propagation stage.
- Carry logic block gets very complicated for more than 4-bits.
- Section-carry based CLAs (SCBCLAs) were proposed as an alternative to conventional CLAs for a 32-bit addition operation, the SCBCLA was found to exhibit reduced propagation delay than the conventional CLA by 15.2%.
- In conventional CLA all the four carries generated by carry logic block are used but in Section-carry based CLAs (SCBCLAs) only the last carry i.e C_4 generated by CLB is used for sum generation.
- As in SCBCLA the concentration is only on last carry generated so propagation delay of SCBCLA gets reduced than conventional CLA.

Carry Select Adder (CSLA)



(b) 8-bit conventional CSLA comprising full adders and 2:1 MUXes (CSLA type)[1]

- Fig shows the 8- bits conventional carry select adder.
- The carry select adder generally consist of two RCA and muiltiplxer. Here the input partitioning is used i.e the least significant 4- bits were generated using RCA method and MSB 4- bits using CSLA.
- The carry generated by 4-bits RCA is served as select input for mux.
- As two RCA were used for MSB 4-bits the sum will be generated on basis of carry input selected.
- Carry Select Adder (CSLA) architecture consists of independent generation of sum and carry i.e., Cin=1 and Cin=0 are executed parallely. Depending upon Cin , the external multiplexers select the carry to be propagated to next stage.
- Further, based on the carry input, the sum will be selected. Hence, the delay is reduced.

2. Literature Review

V. Kokilavani, K. Preethi and P. Balasubramanian[1] In this paper proposed, existing CSLA architectures viz. homogeneous and heterogeneous have been described and two new hybrid CSLA topologies were put forward: (i) carry selectcum- section-carry based carry lookahead adder (CSLASCBCLA) and (ii) carry select-cum-section-carry based carry lookahead adder including BEC logic (CSLA BECSCBCLA). The speed performances of the various CSLA structures have been analyzed based on the case studies of 32-bit and 64-bit dual-operand and multioperand additions. Both uniform and non uniform input data partitions were considered for the various CSLA implementations and FPGA-based synthesis was performed. It has been found for dual-operand additions; the proposed CSLASCBCLA/CSLA BEC-SCBCLA architecture is faster and outperforms all other homogeneous and heterogeneous CSLAs. For bit-partitioned multi-input additions, the proposed CSLA-SCBCLA/CSLA BEC-SCBCLA architecture promises high speed. Nevertheless, for multioperand addition based on the CSA topology, the conventional CSLA BEC-CLA and the proposed CSLA BEC-SCBCLA architectures were found to exhibit an optimized and comparable speed performance. From the inferences derived through this work, it is likely that the proposed hybrid CSLA architectures could achieve enhanced performance over conventional CSLAs for ASIC based synthesis as well. **Ms. S.Manjui, Mr. V. Sornagopae[2]** proposed a simple approach to reduce the area, power and delay of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area, total power and also reduces the delay. A regular CSLA uses two copies of the carry evaluation blocks, one with block carry input is zero and other one with block carry input is one. The Regular SQRT CSLA has the disadvantage of more power consumptions and occupying more chip area. The modified SQRT CSLA reduces the area and power when compared to regular CSLA with increase in delay by the use of Binary to Excess-I converter. This paper proposes a scheme which reduces the delay, area and power than regular and modified CSLA by the use of Common Boolean Logic.**K. Preethi, P. Balasubramanian[3]** Present a FPGA based realization of high-speed carry look-ahead adders based on the concept of section-carry is discussed. A variety of CLA adders belonging to both CCLA and SCBCLA types of sizes 16, 32 and 64-bits were constructed in a topological sense using Verilog HDL and were subsequently synthesized by targeting a 90nm FPGA device (Spartan 3E –XC3S1600E). In comparison with conventional carry look-ahead adders of sizes 16, 32 and 64-bits, the proposed section-carry based carry look-ahead adders report improvements in speed.

3. Proposed Work

Initially different adders currently used in different applications were studied thoroughly. Comparative study for different adders on basis of minimum area, power and delay has been done. Then three different adders will be implemented for minimum area. power and delay. Reconfigured the above three adders at runtime and load the specific adder according to application.

4. References

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